1. ALL RESISTANCE VALUES ARE IN OHMS, 0.1 WATT +/- 5%.
2. ALL CAPACITANCE VALUES ARE IN MICROFARADS.
3. ALL CRYSTALS & OSCILLATOR VALUES ARE IN HERTZ.

REV	ECN	DESCRIPTION OF REVISION	CK APPD / DATE
			2010-08-05

SCHEM,FLYING_CLOUD,MLB,K90i

"EVT3" 11/22/10

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14	16	CPU DECOUPLING-I	JACK_K90I	06/28/2010
15	17	CPU DECOUPLING-II	JACK_K90I	06/28/2010
16	18	PCH SATA/PCIE/CLK/LPC/SPI	K91_MLB	06/18/2010
17	19	PCH DMI/FDI/GRAPHICS	K91_MLB	06/18/2010
18	20	PCH PCI/FLASHCACHE/USB	K91_MLB	06/10/2010
19	21	PCH MISC	K91_MLB	06/18/2010
20	22	PCH POWER	K91_MLB	06/25/2010
21	23	PCH GROUNDS	K91_MLB	05/27/2010
22	24	PCH DECOUPLING	K91_MLB	06/25/2010
23	25	CPU & PCH XDP	ANNE_K90I	06/22/2010
24	26	USB HUBS	K91_MLB	06/08/2010
25	27	Clock (CK505)	K91_MLB	06/21/2010
26	28	Chipset Support	LINDA_K90I	07/08/2010
27	29	DDR3 SO-DIMM Connector A	MASTER	MASTER
28	30	DDR3 Byte/Bit Swaps	ANNE_K90I	06/22/2010
29	31	DDR3 SO-DIMM Connector B	MASTER	MASTER
30	32	CPU Memory S3 Support	ANNE_K90I	06/22/2010
31	33	FSB/DDR3/FRAMEBUF Vref Margining	K91_MLB	06/01/2010
32	34	X19/ALS/CAMERA CONNECTOR	K91_MLB	05/15/2010
33	35	SD READER CONNECTOR	K91_MLB	05/26/2010
34	36	T29 Host (1 of 2)	T29	10/12/2010
35	37	T29 Host (2 of 2)	T29	10/12/2010
36	38	T29 Power Support	T29	10/12/2010
37	39	ETHERNET PHY (CAESAR IV)	K91_MLB	05/26/2010
38	40	Ethernet Connector	K91_MLB	05/26/2010
39	41	FireWire LLC/PHY (FW643E)	T27_MLB	07/20/2009
40	42	FireWire Port & PHY Power	T27_MLB	12/15/2009
41	43	FireWire Connector	T27_MLB	07/28/2009
42	45	SATA/IR/SIL Connectors	K91_MLB	05/15/2010
43	46	External USB Connectors	K91_MLB	06/01/2010
44	48	Front Flex Support	K91_MLB	05/15/2010
45	49	SMC	LINDA_K90I	07/07/2010
46	50	SMC Support	LINDA_K90I	07/08/2010
47	51	LPC+SPI Debug Connector	K91_MLB	05/15/2010
48	52	SMBus Connections	K91_MLB	05/26/2010
49	53	Voltage & Load Side Current Sensing	LINDA_K90I	10/22/2010
50	54	High Side Current Sensing	LINDA_K90I	10/22/2010
51	55	Thermal Sensors	LINDA_K90I	10/22/2010
52	56	Fan	K24_MLB	07/20/2009
53	57	WELLSPRING 1	LINDA_K90I	07/12/2010
54	58	WELLSPRING 2	LINDA_K90I	07/12/2010
55	59	Digital Accelerometer	LINDA_K90I	07/08/2010
56	61	SPI ROM	K91_MLB	05/15/2010
57	62	AUDIO: CODEC/REGULATOR	LENG_K90I	08/10/2010
58	63	AUDIO: LINE INPUT FILTER	LENG_K90I	08/10/2010
59	65	AUDIO: HEADPHONE FILTER	LENG_K90I	08/10/2010
60	66	AUDI0: SPEAKER AMP	LENG_K90I	08/10/2010
61	67	AUDIO: JACK	LENG_K90I	08/10/2010
62	68	AUDIO: JACK TRANSLATORS	LENG_K90I	08/10/2010
63	69	DC-In & Battery Connectors	JACK_K90I	08/20/2010
64	70	PBus Supply & Battery Charger	JACK_K90I	10/11/2010
65	71	System Agent Supply	JACK_K90I	08/19/2010
66	72	5V/3.3V SUPPLY	JACK_K90I	10/04/2010
67	73	1.5V DDR3 Supply	JACK_K90I	10/11/2010
68	74	CPU IMVP7 & AXG VCore Regulator	JACK_K90I	10/14/2010
69	75	CPU IMVP7 & AXG VCore Output	JACK_K90I	09/03/2010
70	76	CPUVCCIO (1.05V) Power Supply	JACK_K90I	08/19/2010
71	77	Misc Power Supplies	JACK_K90I	08/19/2010
72	78	Power FETs	JACK_K90I	10/22/2010
73	79	Power Control 1/ENABLE	JACK_K90I	10/22/2010
74	90	LVDS CONNECTOR	K24_MLB	07/20/2009
75	93	DisplayPort/T29 A MUXing	T29	10/16/2010
76	94	DisplayPort/T29 A Connector	T29	10/16/2010
77	97	LCD Backlight Driver	VEMURI_K90I	06/25/2010
78	100	CPU Constraints	ANNE_K90I	06/08/2010
79	101	Memory Constraints	ANNE_K90I	05/28/2010
80	102	PCH Constraints 1	K91_MLB	05/15/2010
81	103	PCH Constraints 2	K91_MLB	05/15/2010
82	104	Ethernet/FW Constraints	K91_MLB	05/15/2010
83	105	T29 Constraints	Master	06/21/2010
84	106	SMC Constraints	K91_MLB	05/15/2010
85	108	Project Specific Constraints	ANNE_K90I	06/08/2010
86	109	PCB Rule Definitions	ANNE_K90I	06/08/2010

ALIASES RESOLVED

Schematic / PCB #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
051-8658	1	SCHEM,MLB,K90i	SCH	CRITICAL	
820-2936	1	PCBF,MLB,K90i	PCB	CRITICAL	

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TITLE=MLB
ABBREV=DRAWING
LAST_MODIFIED=Mon Nov 22 19:21:11 2010

DRAWING TITLE: SCHEM,FLYING CLOUD,MLB,K90i

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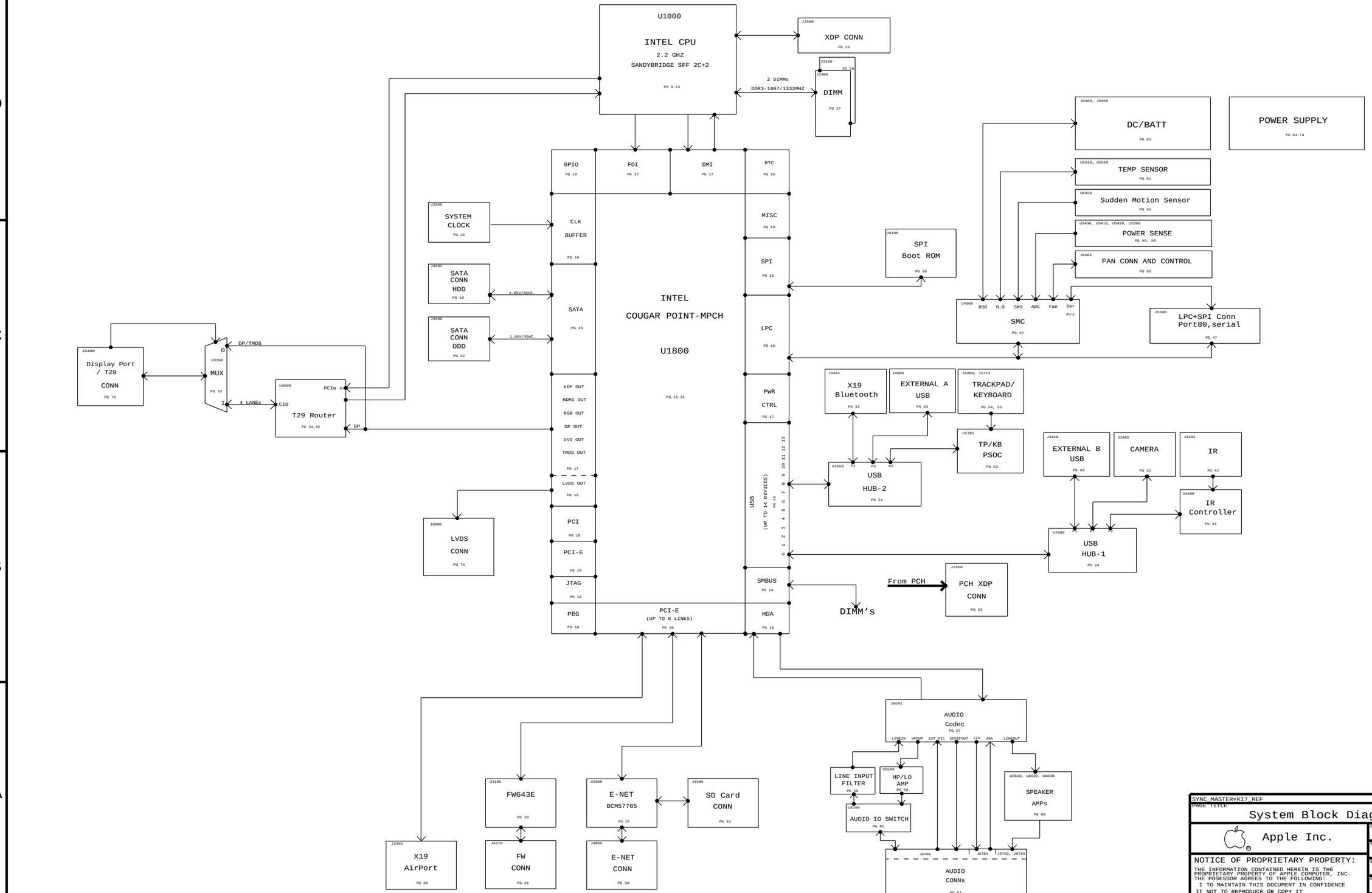

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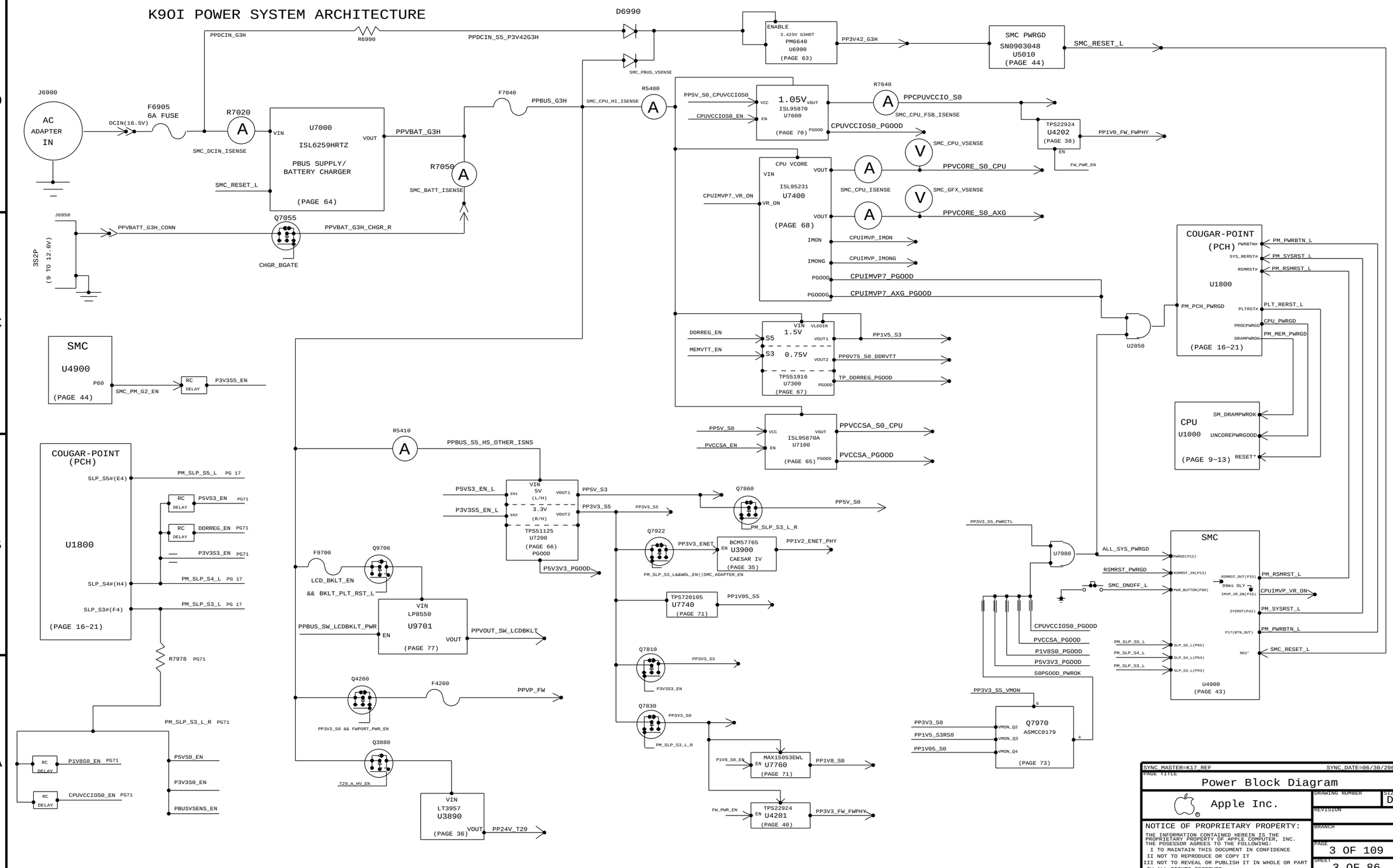
K90I POWER SYSTEM ARCHITECTURE



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BOM Variants

BOM NUMBER	BOM NAME	BOM OPTIONS
639-1294	PCBA,2.5G,K90i	K90i_COMMON,CPU_2_5GHZ,EEEE_DDRQ
639-1581	PCBA,2.7G,K90i	K90i_COMMON,CPU_2_7GHZ,EEEE_DH78
639-1698	PCBA,2.6G,K90i	K90i_COMMON,CPU_2_6GHZ,EEEE_DH8F
639-1699	PCBA,2.3G,K90i	K90i_COMMON,CPU_2_3GHZ,EEEE_DH8G
085-1998	K90i MLB DEVELOPMENT BOM	K90i_DEVEL:ENG

K90i BOM GROUPS

BOM GROUP	BOM OPTIONS
K90i_COMMON	ALTERNATE,COMMON,K90i_COMMON1,K90i_COMMON2,K90i_DEBUG:ENG,K90i_PROGPARTS,USBHUB_2513B,T29BST:Y
K90i_COMMON1	BATT_3S,CPUMEM_S0,SMC_DEBUG_YES,HUB1_2NONREM,HUB2_3NONREM,T29:YES,DP_SDRV:A2,SDRV_PD,SDRVI2C:MCU
K90i_COMMON2	MIKEY,KB_BL
K90i_PROGPARTS	BOOTROM_PROG,SMC_PROG,TPAD_PROG,ENET_PROG,T29ROM:PROG,T29MCU:PROG
K90i_DEVEL:ENG	BKLT:ENG,BMON:ENG,XDP_CONN,XDP_CPU:BPM,XDP_PCH,LPCPLUS,VREFMRGN,S0PGOOD_ISL,IMVPISNS_ENG
K90i_DEVEL:PVT	LPCPLUS,XDP_CONN,XDP_PCH
K90i_DEBUG:ENG	DEVEL_BOM,SMC_DEBUG_YES,XDP
K90i_DEBUG:PVT	DEVEL_BOM,BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT
K90i_DEBUG:PROD	BKLT:PROD,BMON:PROD,SMC_DEBUG_YES,XDP,VREFMRGN_NOT,LPCPLUS

Module Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
337S3934	1	SNB,2C,QXXX,ES1,2.2,35W,B2,3M,GT1,BGA	U1000	CRITICAL	CPU_2_2GHZ
337S4058	1	SNB,Q1RA,QS,J1,2.5,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_5GHZ
337S4057	1	SNB,Q1R3,QS,J1,2.7,35W,2+2,1.30,4M,BGA	U1000	CRITICAL	CPU_2_7GHZ
337S4024	1	SNB,Q1R9,QS,J1,2.3,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_3GHZ
337S4064	1	SNB,Q1R7,QS,J1,2.6,35W,2+2,1.30,3M,BGA	U1000	CRITICAL	CPU_2_6GHZ
337S4029	1	IC,PCH,COUGARPOINT,SLH9D,PRQ,BD82HM65	U1800	CRITICAL	
343S0534	1	IC,BCM57765B0,ENET&SD,8X8	U3900	CRITICAL	
338S0753	1	IC,FW643-E2,1394B PHY/DHCI LINK/PCI-E,32	U4100	CRITICAL	
338S0921	1	IC,T29-C0,220 FCBGA,15x15MM	U3600	CRITICAL	T29:YES
353S3055	1	IC,PI3VEDP212,X2 DISPLAYPORT 2:1 MUX,QFN	U9390	CRITICAL	

Programmable Parts

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
335S0663	1	IC,FLASH,SERIAL,SPI,!MBIT,2V7,BP,SOIC	U3990	CRITICAL	ENET_BLANK
341S3026	1	IC ENET,1!MBITFLAH,CIV REV01,K60/K62	U3990	CRITICAL	ENET_PROG
335S0777	1	IC,EEPROM,SERIAL,SPI,1Kx8,1.8V,MLP8,LF	U3690	CRITICAL	T29ROM:BLANK
341T0317	1	IC,T29 ASSY	U3690	CRITICAL	T29ROM:PROG
337S3997	1	IC,MCU,32B,LPC1112A,16KB/2KB,HVQFN25	U9330	CRITICAL	T29MCU:BLANK
341S2939	1	IC,PROGRMD,LPC1112A,T29 PORT MCU,HVQFN25	U9330	CRITICAL	T29MCU:PROG
338S0895	1	IC,SMC,HS8/2117/9MMx9MM,TLP	U4900	CRITICAL	SMC_BLANK
341T0300	1	IC,SMC,K90i	U4900	CRITICAL	SMC_PROG
335S0770	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
335S0769	1	64 MBIT SPI SERIAL DUAL I/O FLASH	U6100	CRITICAL	BOOTROM_BLANK
341T0299	1	IC,EFI ROM,K90i	U6100	CRITICAL	BOOTROM_PROG
341S2384	1	IR,ENCORE II, CY7C63803-LQXC	U4800	CRITICAL	
341S3024	1	IC,TP PSOC,K90,K90i,K91,K91F,K92	U5701	CRITICAL	TPAD_PROG

Development BOM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
085-1998	1	K90i MLB DEVELOPMENT	DEVEL	CRITICAL	DEVEL_BOM

Bar Code Labels / EEEE #'s

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DDRQ]	CRITICAL	EEEE_DDRQ
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DH78]	CRITICAL	EEEE_DH78
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DH8F]	CRITICAL	EEEE_DH8F
826-4393	1	LBL,P/N LABEL,PCB,28MM X 6 MM	[EEEE:DH8G]	CRITICAL	EEEE_DH8G

Alternate Parts

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
138S0603	138S0602		ALL	Murata alt to Samsung
157S0058	157S0055		ALL	Delta alt to TDK Magnetics
516S0805	516S0806		ALL	Molex alt to Foxconn
128S0303	128S0282		ALL	Panasonic alt to Sanyo
138S0676	138S0691		ALL	Murata alt to Samsung
152S0778	152S0693		ALL	Cyntec alt to Vishay
376S0855	376S0613		ALL	Diodes alt to Toshiba
376S0977	376S0859		ALL	Diodes alt to Toshiba
376S0972	376S0612		ALL	Rohm alt to Toshiba
376S0927	376S0966		ALL	Fairchild alt to Renesas
376S0927	376S0790		ALL	Fairchild alt to CICLON
376S0960	376S0801		ALL	Renesas alt to Renesas
376S0790	376S0928		ALL	CICLON alt to Fairchild
376S0928	376S0895		ALL	Fairchild alt to Renesas
376S0937	376S0845		ALL	Fairchild alt to Renesas
376S0777	376S0761		ALL	AON alt to Siliconix
376S0957	376S0958		ALL	Fairchild alt to Fairchild
376S0953	376S0958		ALL	Fairchild alt to Renesas
353S3085	353S1658		ALL	STmicro alt to LT

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BOM Configuration

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Functional Test Points

Fan Connectors

1815	TRUE	PP5V_S0	6 7 22 42 47 52 54 65 68 70 72 73 77
1816	TRUE	FAN_RT_PWM	52
1817	TRUE	FAN_RT_TACH	52

(NEED TO ADD 1 GND TP)

MIC FUNC_TEST

1635	TRUE	BI_MIC_LO	61 62
1636	TRUE	BI_MIC_HI	61 62
1606	TRUE	BI_MIC_SHIELD	61 62

(NEED TO ADD 1 GND TP)

SPEAKER FUNC_TEST

1227	TRUE	SPKRAMP_L_N_OUT	60 61 85
1225	TRUE	SPKRAMP_L_P_OUT	60 61 85
1223	TRUE	SPKRAMP_R_N_OUT	60 61 85
1230	TRUE	SPKRAMP_R_P_OUT	60 61 85
1229	TRUE	SPKRAMP_SUB_N_OUT	60 61 85
1231	TRUE	SPKRAMP_SUB_P_OUT	60 61 85

LVDS FUNC_TEST

1202	TRUE	PP3V3_LCDVDD_SW_F (NEED 2 TP)	
1203	TRUE	PP3V3_S0_LCD_F	6 74
1204	TRUE	PPVOUT_SW_LCDBKLT (NEED 2 TP)	74 77
1640	TRUE	BKL_VSYNC	74 77
1410	TRUE	LVDS_DDC_CLK	8 18 74
1409	TRUE	LVDS_DDC_DATA	8 18 74
1943	TRUE	LVDS_IG_A_DATA_N<0>	18 74 80
1944	TRUE	LVDS_IG_A_DATA_P<0>	18 74 80
1947	TRUE	LVDS_IG_A_DATA_N<1>	18 74 80
1948	TRUE	LVDS_IG_A_DATA_P<1>	18 74 80
1950	TRUE	LVDS_IG_A_DATA_N<2>	18 74 80
1949	TRUE	LVDS_IG_A_DATA_P<2>	18 74 80
1914	TRUE	LVDS_CONN_A_CLK_F_N	74 85
1916	TRUE	LVDS_CONN_A_CLK_F_P	74 85
1951	TRUE	LED_RETURN_1	74 77
1913	TRUE	LED_RETURN_2	74 77
1946	TRUE	LED_RETURN_3	74 77
1945	TRUE	LED_RETURN_4	74 77
1938	TRUE	LED_RETURN_5	74 77
1939	TRUE	LED_RETURN_6	74 77

(NEED TO ADD 5 GND TP)

SATA ODD CONN

1264	TRUE	PP5V_SW_ODD (NEED 2 TP)	6 42
1265	TRUE	SMC_ODD_DETECT	42 45
1266	TRUE	SATA_ODD_D2R_UF_P	42 85
1267	TRUE	SATA_ODD_D2R_UF_N	42 85
1268	TRUE	SATA_ODD_R2D_P	42 80
1269	TRUE	SATA_ODD_R2D_N	42 80

(NEED TO ADD 3 GND TP)

SATA HDD/IR/SIL

1312	TRUE	PP5V_S0_HDD_FLT (NEED 2 TP)	6 42
1314	TRUE	SATA_HDD_R2D_P	42 80
1315	TRUE	SATA_HDD_R2D_N	42 80
1316	TRUE	SATA_HDD_D2R_C_P	42 80
1317	TRUE	SATA_HDD_D2R_C_N	42 80
1307	TRUE	SYS_LED_ANODE_R	42
1302	TRUE	IR_RX_OUT	42 44
1311	TRUE	PP5V_S3_IR_R	42

(NEED TO ADD 3 GND TP)

BATT POWER CONN

1322	TRUE	SMBUS_SMC_BSA_SCL	6 45 48 63 64 84
1323	TRUE	SMBUS_SMC_BSA_SDA	6 45 48 63 64 84
1326	TRUE	SYS_DETECT_L	63
1305	TRUE	PPVBAT_G3H_CONN (NEED 5 TP)	63 64

(NEED TO ADD 5 GND TP)

BIL CONN

1325	TRUE	PP3V42_G3H	6 7 26 43 45 46 47 48 53 63 64 73
1322	TRUE	SMBUS_SMC_BSA_SCL	6 45 48 63 64 84
1324	TRUE	SMBUS_SMC_BSA_SDA	6 45 48 63 64 84
1329	TRUE	SMC_BIL_BUTTON_L	45 46 63
1328	TRUE	SMC_LID_R	63

(NEED TO ADD 2 GND TP)

X19 CONN

1902	TRUE	PP3V3_WLAN (NEED 3 TP)	6 32 46
1903	TRUE	PCIE_AP_D2R_PI_P	32 81
1904	TRUE	PCIE_AP_D2R_PI_N	32 81
1905	TRUE	PCIE_AP_R2D_P	32 81
1906	TRUE	PCIE_AP_R2D_N	32 81
1908	TRUE	PCIE_CLK100M_AP_CONN_P	32 85
1909	TRUE	PCIE_CLK100M_AP_CONN_N	32 85
1910	TRUE	PP3V3_S3_BT_F	32
1911	TRUE	PCIE_WAKE_L	17 26 32
1912	TRUE	SMBUS_SMC_0_S0_SCL	32 45 48 51 84
1913	TRUE	SMBUS_SMC_0_S0_SDA	32 45 48 51 84
1914	TRUE	USB_BT_P	24 32 80
1915	TRUE	USB_BT_N	24 32 80
1916	TRUE	AP_CLKREQ_O_L	32
1917	TRUE	AP_RESET_CONN_L	32
1918	TRUE	AP_TEMP_SMB_SDA_R	32
1919	TRUE	AP_TEMP_SMB_SCL_R	32
1920	TRUE	WIFI_EVENT_L_R	32

(NEED TO ADD 5 GND TP)

IPD_FLEX_CONN

1373	TRUE	PP3V3_S5	76 85 6 7 8 17 19 20 22 23 24 26 30 46 56 66 72 73 74 76 85
1374	TRUE	PP18V5_S5	6 54
1377	TRUE	Z2_CS_L	53 54
1378	TRUE	Z2_DEBUG3	53 54
1371	TRUE	Z2_MOSI	53 54
1369	TRUE	Z2_MISO	53 54
1368	TRUE	Z2_SCLK	53 54
1367	TRUE	Z2_BOOST_EN	54
1366	TRUE	Z2_HOST_INTN	53 54
1365	TRUE	Z2_CLKIN	53 54
1363	TRUE	Z2_KEY_ACT_L	53 54
1364	TRUE	Z2_RESET	53 54
1362	TRUE	PSOC_MISO	53 54
1360	TRUE	PSOC_MOSI	53 54
1359	TRUE	PSOC_SCLK	53 54
1361	TRUE	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55 84
1358	TRUE	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55 84
1357	TRUE	PSOC_F_CS_L	53 54
1606	TRUE	PICKB_L	53 54

(NEED TO ADD 2 GND TP)

KEYBOARD CONN

1354	TRUE	PP3V3_S5	6 7 8 17 19 20 22 23 24 26 30 46 56 66 72 73 74 76 85
1355	TRUE	PP3V42_G3H	6 7 26 43 45 46 47 48 53 63 64 73
1344	TRUE	WS_KBD1	53
1345	TRUE	WS_KBD2	53
1346	TRUE	WS_KBD3	53
1347	TRUE	WS_KBD4	53
1348	TRUE	WS_KBD5	53
1349	TRUE	WS_KBD6	53
1350	TRUE	WS_KBD7	53
1351	TRUE	WS_KBD8	53
1352	TRUE	WS_KBD9	53
1353	TRUE	WS_KBD10	53
1327	TRUE	WS_KBD11	53
1328	TRUE	WS_KBD12	53
1329	TRUE	WS_KBD13	53
1343	TRUE	WS_KBD14	53
1342	TRUE	WS_KBD15_CAP	53
1341	TRUE	WS_KBD16_NUM	53
1339	TRUE	WS_KBD17	53
1340	TRUE	WS_KBD18	53
1338	TRUE	WS_KBD19	53
1336	TRUE	WS_KBD20	53
1337	TRUE	WS_KBD21	53
1331	TRUE	WS_KBD22	53
1333	TRUE	WS_KBD23	53
1334	TRUE	WS_KBD_ONOFF_L	53
1332	TRUE	WS_LEFT_SHIFT_KBD	53
1330	TRUE	WS_LEFT_OPTION_KBD	53
1335	TRUE	WS_CONTROL_KBD	53

(NEED TO ADD 2 GND TP)

KBD BACKLIGHT CONN

1356	TRUE	KBDLED_ANODE	54
1294	TRUE	SMC_KDBLED_PRESENT_L	54

(NEED TO ADD 1 GND TP)

CAMERA/ALS CONN

1408	TRUE	PP5V_S3_ALSCAMERA_F	32
1409	TRUE	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55 84
1410	TRUE	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55 84
1297	TRUE	USB_CAMERA_CONN_P	32 80
1298	TRUE	USB_CAMERA_CONN_N	32 80

(NEED TO ADD 2 GND TP)

DEBUG VOLTAGE

1287	TRUE	PPVCORE_S0_CPU	7 9 12 14 49 69
1288	TRUE	PPVCORE_S0_AXG	7 9 12 15 49 69
1436	TRUE	PP1V2_S3_ENET_INTREG	37 71
1289	TRUE	PP1V05_S0	45 68 70 73
1290	TRUE	PP1V5_S3RS0	7 9 10 12 14 16 17 20 22 23 36 40
1291	TRUE	PP1V8_S0	7 10 12 15 30 72 73 85
1292	TRUE	PP3V3_S0	7 14 17 20 22 26 71 29 33 36 37 40
1293	TRUE	PP5V_S0	7 8 12 16 1750 18 19 20 22 23 26 27 31 32 33 34 35 36 37 51 52 54 57 61 65 71 72 74 75 77 85
1272	TRUE	PP3V3_S3	7 9 18 24 26 30 31 32 33 48 50 54 55 72 73
1273	TRUE	PP5V_S3	7 30 32 42 43 44 46 57 59 60 61 66 67 72
1410	TRUE	PPVCCSA_S0_CPU	7 12 15 65
1271	TRUE	PP3V3_S5	16 6
1274	TRUE	PP3V42_G3H	16 6 47 48 53 63 64
1275	TRUE	PPBUS_G3H	6 7 34 43 45 46 16 6 7 8 36 40 49 50 63 64 77
1417	TRUE	PP3V3_ENET	7 26 37 71 73
1272	TRUE	PP3V3_WLAN	6 32 46
1277	TRUE	PP5V_SW_ODD	6 42
1199	TRUE	PP5V_S0_HDD_FLT	6 42
1198	TRUE	PP18V5_S5	6 54
1410	TRUE	PP3V3_S0_LCD_F	6 74
1189	TRUE	PP3V3_LCDVDD_SW_F	6 74
1183	TRUE	PP4V5_AUDIO_ANALOG	57
1410	TRUE	PP1V5_S3	7 27 29 30 67 72
1382	TRUE	SMC_PM_G2_EN	45 73
1506	TRUE	PM_SLP_S4_L	17 30 45 73
1380	TRUE	PM_SLP_S3_L	17 30 45 73

(NEED TO ADD 6 GND TP)

DC POWER CONN

(NEED 3 TP)

1312	TRUE	PP18V5_DCIN_FUSE	63
1304	TRUE	ADAPTER_SENSE	63

(NEED TO ADD 4 GND TP)

LPC+SPI DEBUG_CONN

1656	TRUE	LPC_AD<0>	16 45 47 81
1657	TRUE	LPC_AD<1>	16 45 47 81
1658	TRUE	LPC_AD<2>	16 45 47 81
1659	TRUE	LPC_AD<3>	16 45 47 81
1660	TRUE	LPC_CLK33M_LPCPLUS	26 47 81
1661	TRUE	LPC_FRAME_L	16 45 47 81
1662	TRUE	LPC_PWRDWN_L	17 45 47
1663	TRUE	LPC_SERIRQ	16 45 47
1664	TRUE	LPCPLUS_GPIO	19 47
1665	TRUE	LPCPLUS_RESET_L	26 47 81
1666	TRUE	PM_CLKRUN_L	17 45 47
1667	TRUE	PP3V42_G3H	6 7 26 43 45 46 47 48 53 63 64 73
1668	TRUE	PP5V_S0	6 7 22 42 47 52 54 65 68 70 72 73 77
1669	TRUE	SMC_MD1	45 47
1670	TRUE	SMC_RX_L	43 45 46 47
1671	TRUE	SMC_TCK	45 46 47
1672	TRUE	SMC_TDI	45 46 47
1673	TRUE	SMC_TDO	45 46 47
1674	TRUE	SMC_TMS	45 46 47
1675	TRUE	SMC_TRST_L	45 47
1676	TRUE	SMC_TX_L	43 45 46 47
1677	TRUE	SPI_ALT_CLK	47
1678	TRUE	SPI_ALT_CS_L	47
1679	TRUE	SPI_ALT_MISO	47
1680	TRUE	SPI_ALT_MOSI	47
1681	TRUE	SPIROM_USE_MLB	19 47 56

(NEED TO ADD 2 GND TP)

NC NO_TESTs

NO_TEST

17 6	NC_CRT_IG_BLUE	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_BLUE	6 17
17 6	NC_CRT_IG_GREEN	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_GREEN	6 17
17 6	NC_CRT_IG_RED	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_RED	6 17
17 6	NC_CRT_IG_DDC_CLK	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_DDC_CLK	6 17
17 6	NC_CRT_IG_DDC_DATA	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_DDC_DATA	6 17
17 6	NC_CRT_IG_HSYNC	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_HSYNC	6 17
	NC_CRT_IG_VSYNC	TRUE / MAKE_BASE=TRUE	NC_CRT_IG_VSYNC	6 17
	NC_LVDS_IG_CTRL_CLK	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_CLK	6 18
	NC_LVDS_IG_CTRL_DATA	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_CTRL_DATA	6 18
	NC_PCH_LVDS_VBG	TRUE / MAKE_BASE=TRUE	NC_PCH_LVDS_VBG	6 18
	NC_HDA_SDIN1	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN1	6 9 16
	NC_HDA_SDIN2	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN2	6 16
	NC_HDA_SDIN3	TRUE / MAKE_BASE=TRUE	NC_HDA_SDIN3	6 16
18 6	NC_PCI_PME_L	TRUE / MAKE_BASE=TRUE	NC_PCI_PME_L	6 18
18 6	NC_PCI_CLK33M_OUT3	TRUE / MAKE_BASE=TRUE	NC_PCI_CLK33M_OUT3	6 18
16 6	NC_CLINK_CLK	TRUE / MAKE_BASE=TRUE	NC_CLINK_CLK	6 16
16 6	NC_CLINK_DATA	TRUE / MAKE_BASE=TRUE	NC_CLINK_DATA	6 16
16 6	NC_CLINK_RESET_L	TRUE / MAKE_BASE=TRUE	NC_CLINK_RESET_L	6 16
16 6	NC_PCIE_CLK100M_PEBN	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBN	6 16
16 6	NC_PCIE_CLK100M_PEBP	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PEBP	6 16
39 6	NC_FW643_SDA	TRUE / MAKE_BASE=TRUE	NC_FW643_SDA	6 39
39 6	NC_FW643_SM	TRUE / MAKE_BASE=TRUE	NC_FW643_SM	6 39
39 6	NC_FW643_TCK	TRUE / MAKE_BASE=TRUE	NC_FW643_TCK	6 39
39 6	NC_FW643_TMS	TRUE / MAKE_BASE=TRUE	NC_FW643_TMS	6 39
39 6	NC_FW643_FW620_L	TRUE / MAKE_BASE=TRUE	NC_FW643_FW620_L	6 39
39 6	NC_FW643_VBUF	TRUE / MAKE_BASE=TRUE	NC_FW643_VBUF	6 39
39 6	NC_FW643_OCR10_CTL	TRUE / MAKE_BASE=TRUE	NC_FW643_OCR10_CTL	6 39
39 6	NC_FW643_AVREG	TRUE / MAKE_BASE=TRUE	NC_FW643_AVREG	16 6
39 6	NC_FW643_TDI	TRUE / MAKE_BASE=TRUE	NC_FW643_TDI	16 6
	TP_XDP_PCH_OBSFN_A<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_A<0..1>	23 6
	TP_XDP_PCH_OBSFN_B<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_B<0..1>	23 6
23 6	NC_TP_XDPPCH_HOOK2	TRUE / MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK2	6 23
23 6	NC_TP_XDPPCH_HOOK3	TRUE / MAKE_BASE=TRUE	NC_TP_XDPPCH_HOOK3	6 23
	TP_XDP_PCH_OBSFN_D<0..1>	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_OBSFN_D<0..1>	23 6
23 6	NC_TP_XDP_PCH_HOOK4	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK4	6 23
23 6	NC_TP_XDP_PCH_HOOK5	TRUE / MAKE_BASE=TRUE	NC_TP_XDP_PCH_HOOK5	6 23
16 6	NC_PCH_GPIO64_CLKOUTFLEX0	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO64_CLKOUTFLEX0	6 16
16 6	NC_PCH_GPIO65_CLKOUTFLEX1	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO65_CLKOUTFLEX1	6 16
16 6	NC_PCH_GPIO66_CLKOUTFLEX2	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO66_CLKOUTFLEX2	6 16
16 6	NC_PCH_GPIO67_CLKOUTFLEX3	TRUE / MAKE_BASE=TRUE	NC_PCH_GPIO67_CLKOUTFLEX3	6 16

NC NO_TESTs

NO_TEST

1498	TRUE	NC_FW2_TPBP	39 41
1499	TRUE	NC_FW2_TPBN	39 41
1500	TRUE	NC_FW2_TPBIAS	39 41
1497	TRUE	NC_FW2_TPAP	39 41
1496	TRUE	NC_FW2_TPAN	39 41
1495	TRUE	NC_FW0_TPBP	39 41 82
1494	TRUE	NC_FW0_TPBN	39 41 82
1493	TRUE	NC_FW0_TPAP	39 41 82
1492	TRUE	XDP_PCH_AP_PWR_EN	
1491	TRUE	XDP_PCH_USB_HUB_SOFT_RST_L	23
1513	TRUE	XDP_PCH_SDCONN_STATE_RST_L	23
1488	TRUE	XDP_PCH_ENET_PWR_EN	23
1512	TRUE	XDP_PCH_SDCONN_DET_L	23
1489	TRUE	XDP_PCH_S5_PWRGD	23
1484	TRUE	XDP_PCH_PWRBTN_L	23
1485	TRUE	XDP_PCH_ISOLATE_CPU_MEM_L	23
1486	TRUE	XDP_FW_CLKREQ_L	23
1488	TRUE	XDP_AP_CLKREQ_L	23
1487	TRUE	XDP_PCH_AUD_IPHS_SWITCH_EN	23

17 6	NC_SDVO_TVCLKINN	TRUE / MAKE_BASE=TRUE	NC_SDVO_TVCLKINN	6 17
17 6	NC_SDVO_TVCLKINP	TRUE / MAKE_BASE=TRUE	NC_SDVO_TVCLKINP	6 17
17 6	NC_SDVO_STALLN	TRUE / MAKE_BASE=TRUE	NC_SDVO_STALLN	6 17
17 6	NC_SDVO_STALLP	TRUE / MAKE_BASE=TRUE	NC_SDVO_STALLP	6 17
17 6	NC_SDVO_INTN	TRUE / MAKE_BASE=TRUE	NC_SDVO_INTN	6 17
17 6	NC_SDVO_INTP	TRUE / MAKE_BASE=TRUE	NC_SDVO_INTP	6 17

9	NC_EDP_TXP<0..3>	TRUE / MAKE_BASE=TRUE	TP_EDP_TX_P<0..3>	
9	NC_EDP_TXN<0..3>	TRUE / MAKE_BASE=TRUE	TP_EDP_TX_N<0..3>	
9 6	NC_EDP_AUXP	TRUE / MAKE_BASE=TRUE	NC_EDP_AUXP	6 9
9 6	NC_EDP_AUXN	TRUE / MAKE_BASE=TRUE	NC_EDP_AUXN	6 9
6	NC_CPU_THERMDA	TRUE / MAKE_BASE=TRUE	NC_CPU_THERMDA	6
6	NC_CPU_THERMDC	TRUE / MAKE_BASE=TRUE	NC_CPU_THERMDC	6
	NC_CPU_RSVD<30..45>	TRUE / MAKE_BASE=TRUE	TP_CPU_RSVD<30..45>	
	NC_CPU_RSVD<8..27>	TRUE / MAKE_BASE=TRUE	TP_CPU_RSVD<8..27>	
9	NC_PEG_R2D_CP<0..7>	TRUE / MAKE_BASE=TRUE	=PEG_R2D_C_P<0..7>	9
9	NC_PEG_R2D_CN<0..7>	TRUE / MAKE_BASE=TRUE	=PEG_R2D_C_N<0..7>	9
9	NC_PEG_D2RP<0..7>	TRUE / MAKE_BASE=TRUE	=PEG_D2R_P<0..7>	9
9	NC_PEG_D2RN<0..7>	TRUE / MAKE_BASE=TRUE	=PEG_D2R_N<0..7>	9
9	NC_PEG_R2D_CP<12..15>	TRUE / MAKE_BASE=TRUE	=PEG_R2D_C_P<12..15>	
9	NC_PEG_R2D_CN<12..15>	TRUE / MAKE_BASE=TRUE	=PEG_R2D_C_N<12..15>	
9	NC_PEG_D2RP<12..15>	TRUE / MAKE_BASE=TRUE	=PEG_D2R_P<12..15>	
9	NC_PEG_D2RN<12..15>	TRUE / MAKE_BASE=TRUE	=PEG_D2R_N<12..15>	
6	NC_PCIE_CLK100M_PE4N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4N	6
6	NC_PCIE_CLK100M_PE4P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE4P	6
6	NC_PCIE_CLK100M_PE5N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5N	6 16
6	NC_PCIE_CLK100M_PE5P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE5P	6 16
6	NC_PCIE_CLK100M_PE6N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6N	6 19
6	NC_PCIE_CLK100M_PE6P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE6P	6 19
6	NC_PCIE_CLK100M_PE7N	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7N	6 19
6	NC_PCIE_CLK100M_PE7P	TRUE / MAKE_BASE=TRUE	NC_PCIE_CLK100M_PE7P	6 19
53 6	NC_PSOC_P1_3	TRUE / MAKE_BASE=TRUE	NC_PSOC_P1_3	6 53
16 6	NC_SATA_B_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_B_D2RN	6 16
16 6	NC_SATA_B_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_B_D2RP	6 16
16 6	NC_SATA_B_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_B_R2D_CN	6 16
16 6	NC_SATA_B_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_B_R2D_CP	6 16
16 6	NC_SATA_D_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_D_D2RN	6 16
16 6	NC_SATA_D_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_D_D2RP	6 16
16 6	NC_SATA_D_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_D_R2D_CN	6 16
16 6	NC_SATA_D_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_D_R2D_CP	6 16
16 6	NC_SATA_E_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_E_D2RN	6 16
16 6	NC_SATA_E_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_E_D2RP	6 16
16 6	NC_SATA_E_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_E_R2D_CN	6 16
16 6	NC_SATA_E_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_E_R2D_CP	6 16
16 6	NC_SATA_F_D2RN	TRUE / MAKE_BASE=TRUE	NC_SATA_F_D2RN	6 16
16 6	NC_SATA_F_D2RP	TRUE / MAKE_BASE=TRUE	NC_SATA_F_D2RP	6 16
16 6	NC_SATA_F_R2D_CN	TRUE / MAKE_BASE=TRUE	NC_SATA_F_R2D_CN	6 16
16 6	NC_SATA_F_R2D_CP	TRUE / MAKE_BASE=TRUE	NC_SATA_F_R2D_CP	6 16
6	NC_PCH_TP18	TRUE / MAKE_BASE=TRUE	NC_PCH_TP18	6
6	NC_PCH_TP17	TRUE / MAKE_BASE=TRUE	NC_PCH_TP17	6
6	NC_PCH_TP16	TRUE / MAKE_BASE=TRUE	NC_PCH_TP16	6
6	NC_PCH_TP15	TRUE / MAKE_BASE=TRUE	NC_PCH_TP15	6
6	NC_PCH_TP14	TRUE / MAKE_BASE=TRUE	NC_PCH_TP14	6
6	NC_PCH_TP13	TRUE / MAKE_BASE=TRUE	NC_PCH_TP13	6
6	NC_PCH_TP12	TRUE / MAKE_BASE=TRUE	NC_PCH_TP12	6
6	NC_PCH_TP10	TRUE / MAKE_BASE=TRUE	NC_PCH_TP10	6
6	NC_PCH_TP9	TRUE / MAKE_BASE=TRUE	NC_PCH_TP9	6
6	NC_PCH_TP8	TRUE / MAKE_BASE=TRUE	NC_PCH_TP8	6
6	NC_PCH_TP7	TRUE / MAKE_BASE=TRUE	NC_PCH_TP7	6
6	NC_PCH_TP6	TRUE / MAKE_BASE=TRUE	NC_PCH_TP6	6
6	NC_PCH_TP5	TRUE / MAKE_BASE=TRUE	NC_PCH_TP5	6
6	NC_PCH_TP4	TRUE / MAKE_BASE=TRUE	NC_PCH_TP4	6
6	NC_PCH_TP3	TRUE / MAKE_BASE=TRUE	NC_PCH_TP3	6
6	NC_PCH_TP2	TRUE / MAKE_BASE=TRUE	NC_PCH_TP2	6
6	NC_PCH_TP1	TRUE / MAKE_BASE=TRUE	NC_PCH_TP1	6
1522	PCH_VSS_NCTF<1>	TRUE	PCH_VSS_NCTF<15>	81
1523	PCH_VSS_NCTF<2>	TRUE	PCH_VSS_NCTF<17>	81
1520	PCH_VSS_NCTF<5>	TRUE	PCH_VSS_NCTF<19>	6 81
		TRUE	PCH_VSS_NCTF<19>	6 81
		TRUE	PCH_VSS_NCTF<21>	81
1515	PCH_VSS_NCTF<9>	TRUE	PCH_VSS_NCTF<25>	81
1518	PCH_VSS_NCTF<11>	TRUE	PCH_VSS_NCTF<27>	81
1517	PCH_VSS_NCTF<12>	TRUE	PCH_VSS_NCTF<29>	81
80 18 8	TP_LVDS_IG_B_CLKN	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKN	
80 18 8	TP_LVDS_IG_B_CLKP	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_B_CLKP	
6	NC_LVDS_IG_BKL_PWM	TRUE / MAKE_BASE=TRUE	NC_LVDS_IG_BKL_PWM	6
6	NC_SMC_BS_ALRT_L	TRUE / MAKE_BASE=TRUE	NC_SMC_BS_ALRT_L	6

SYNC_MASTER=K24_MLB

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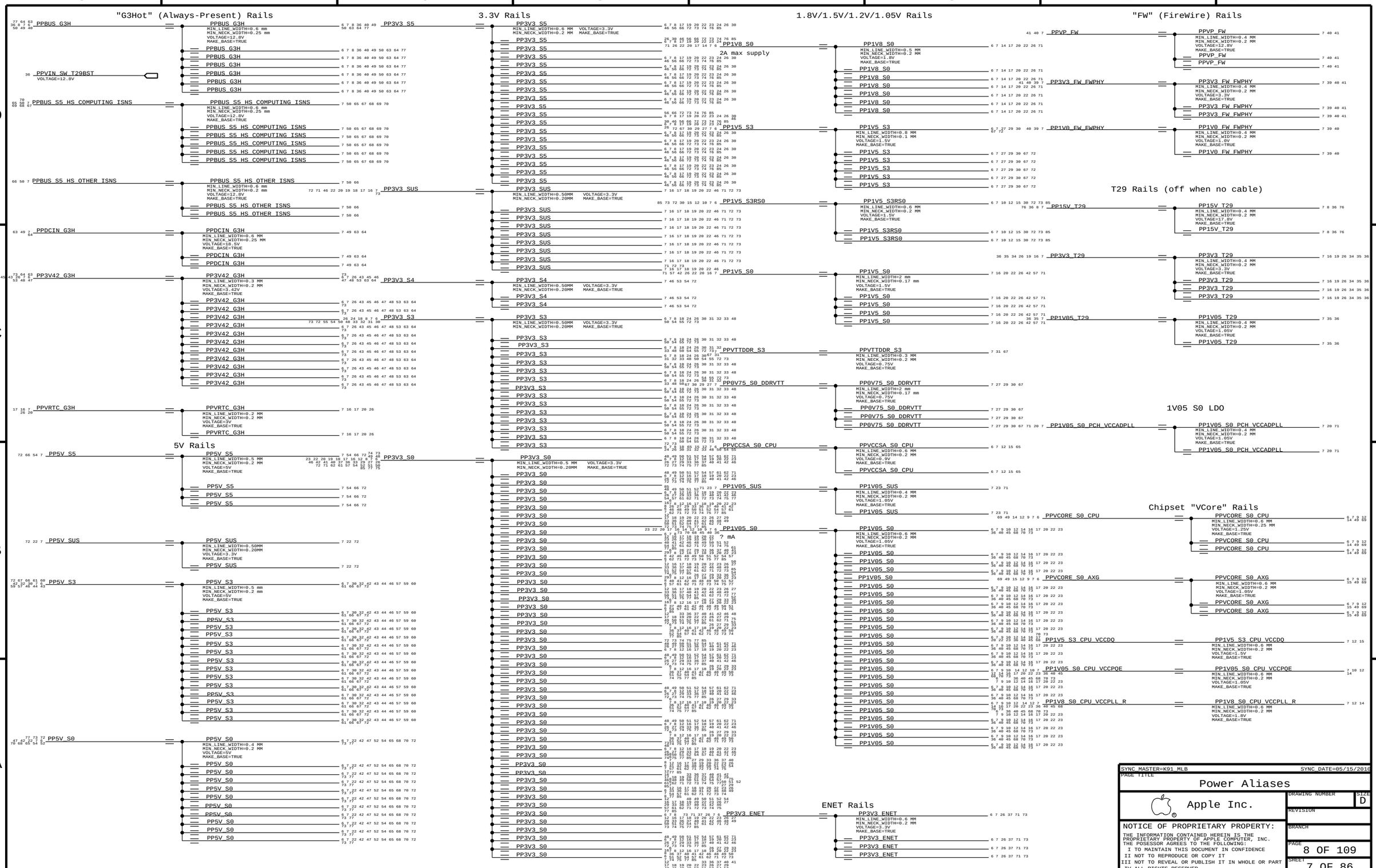

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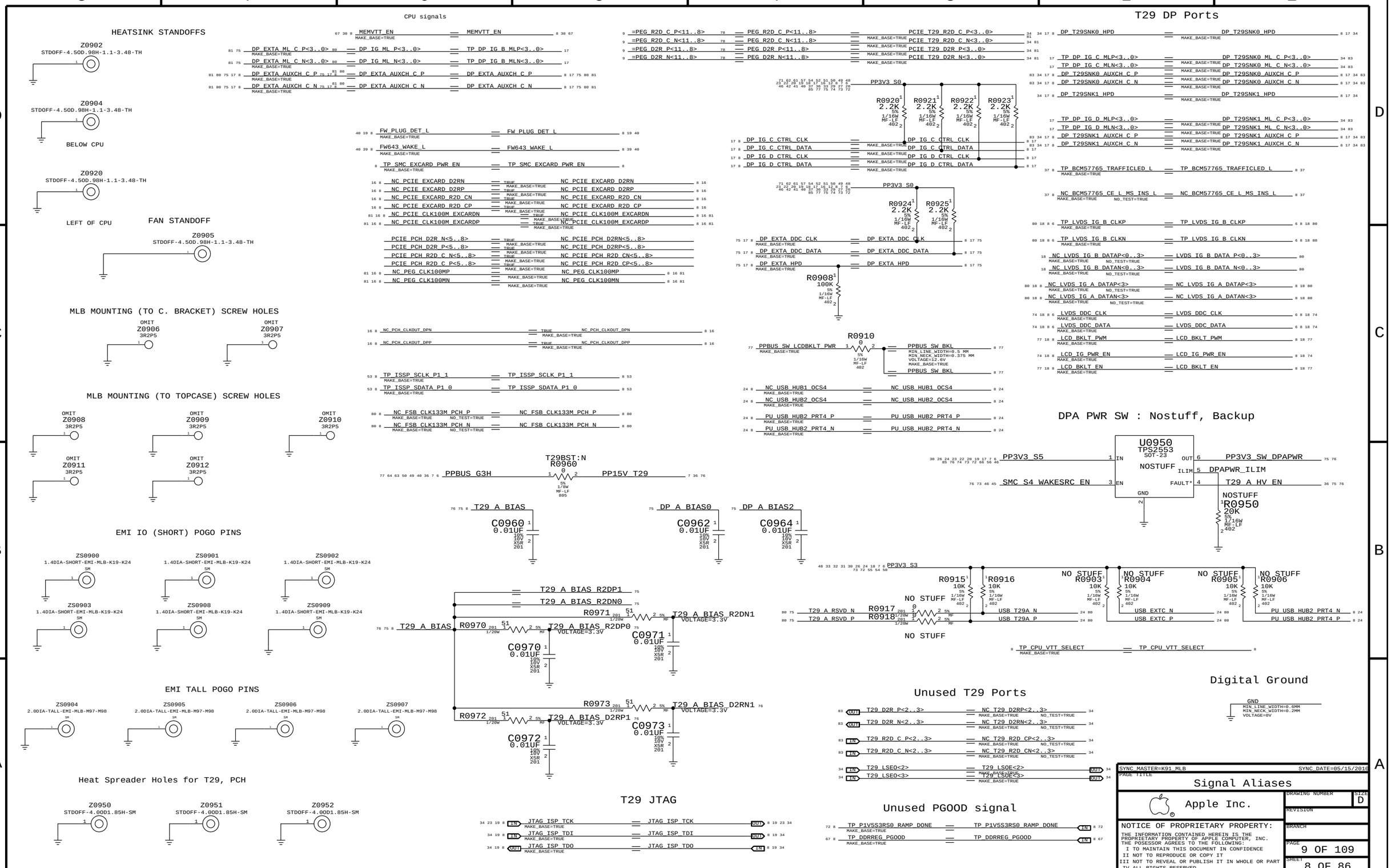

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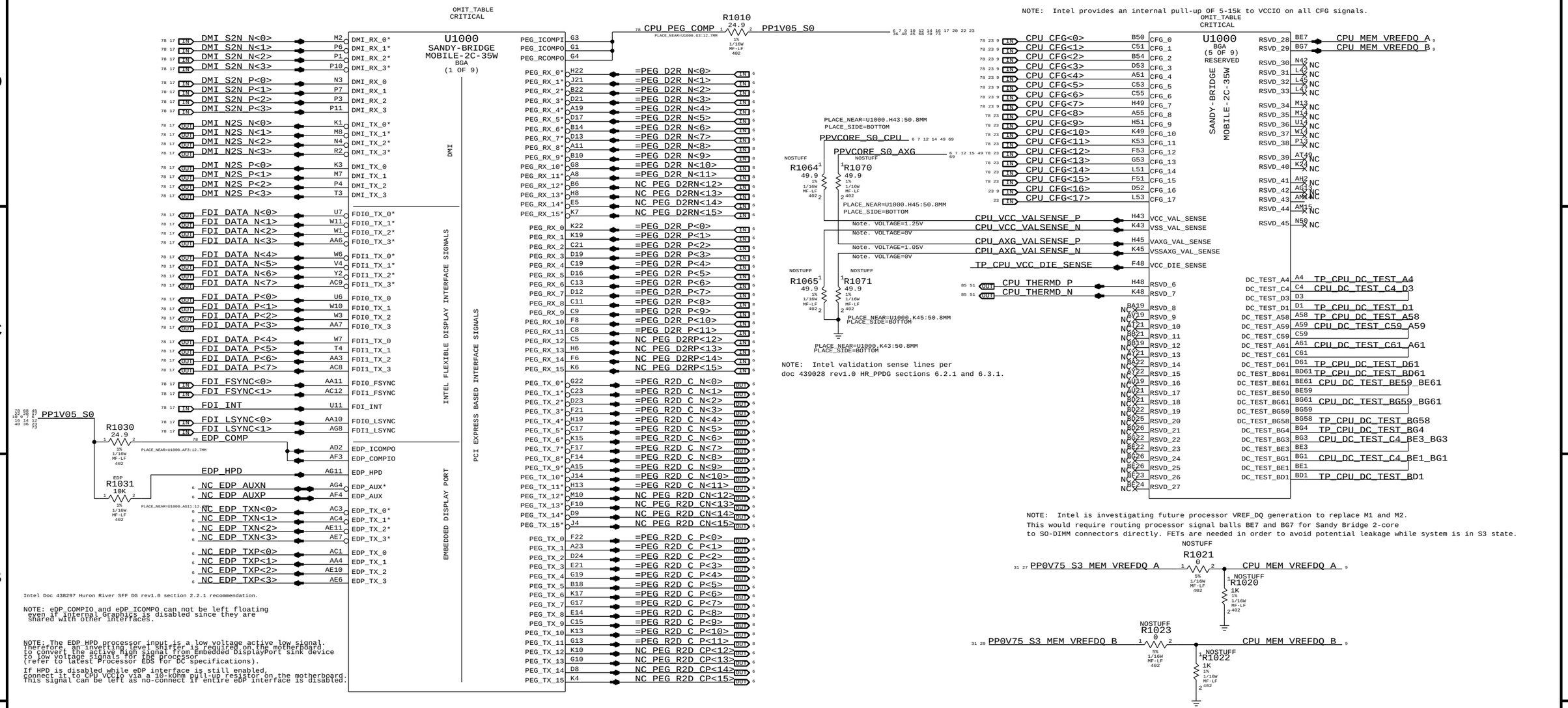

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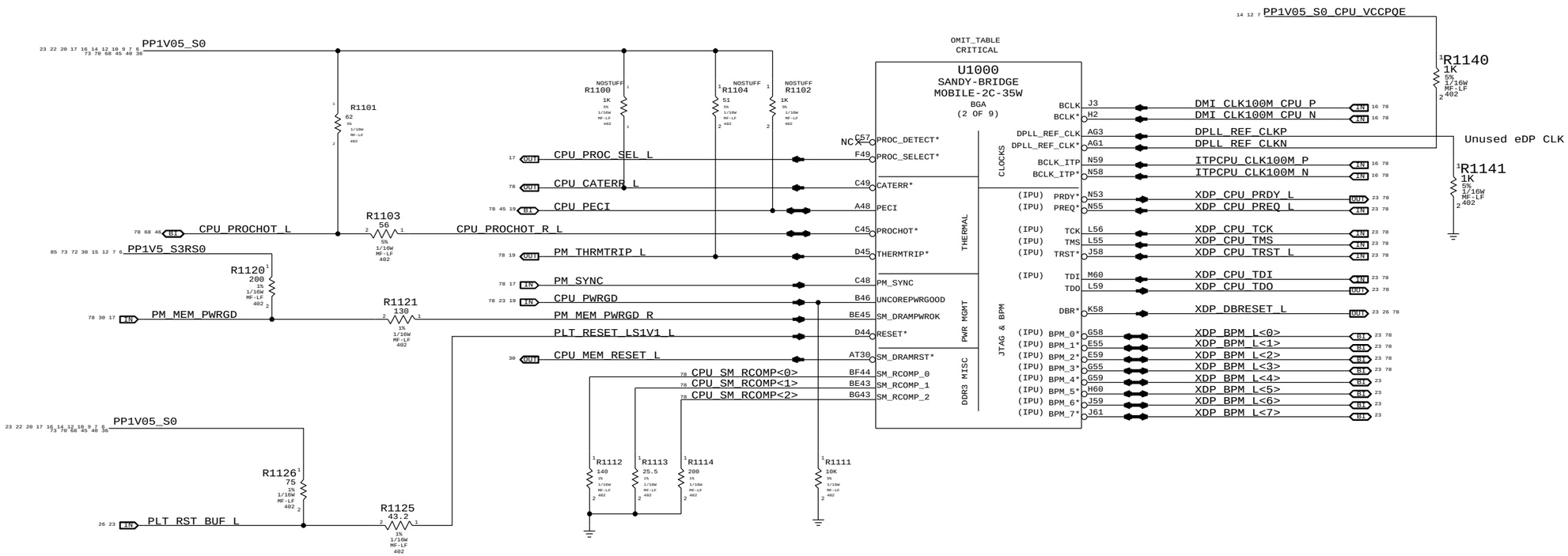

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CPU CLOCK/MISC/JTAG

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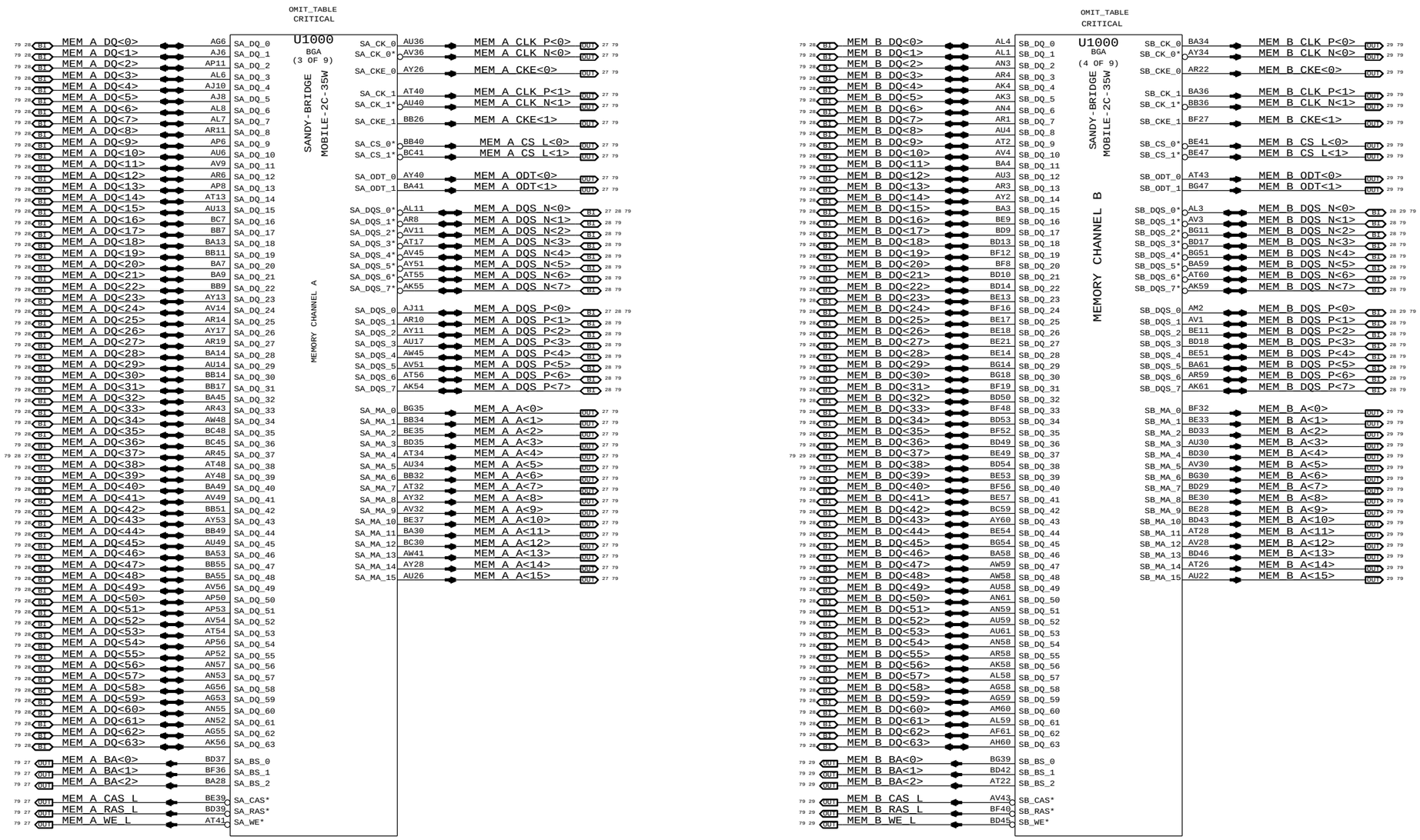

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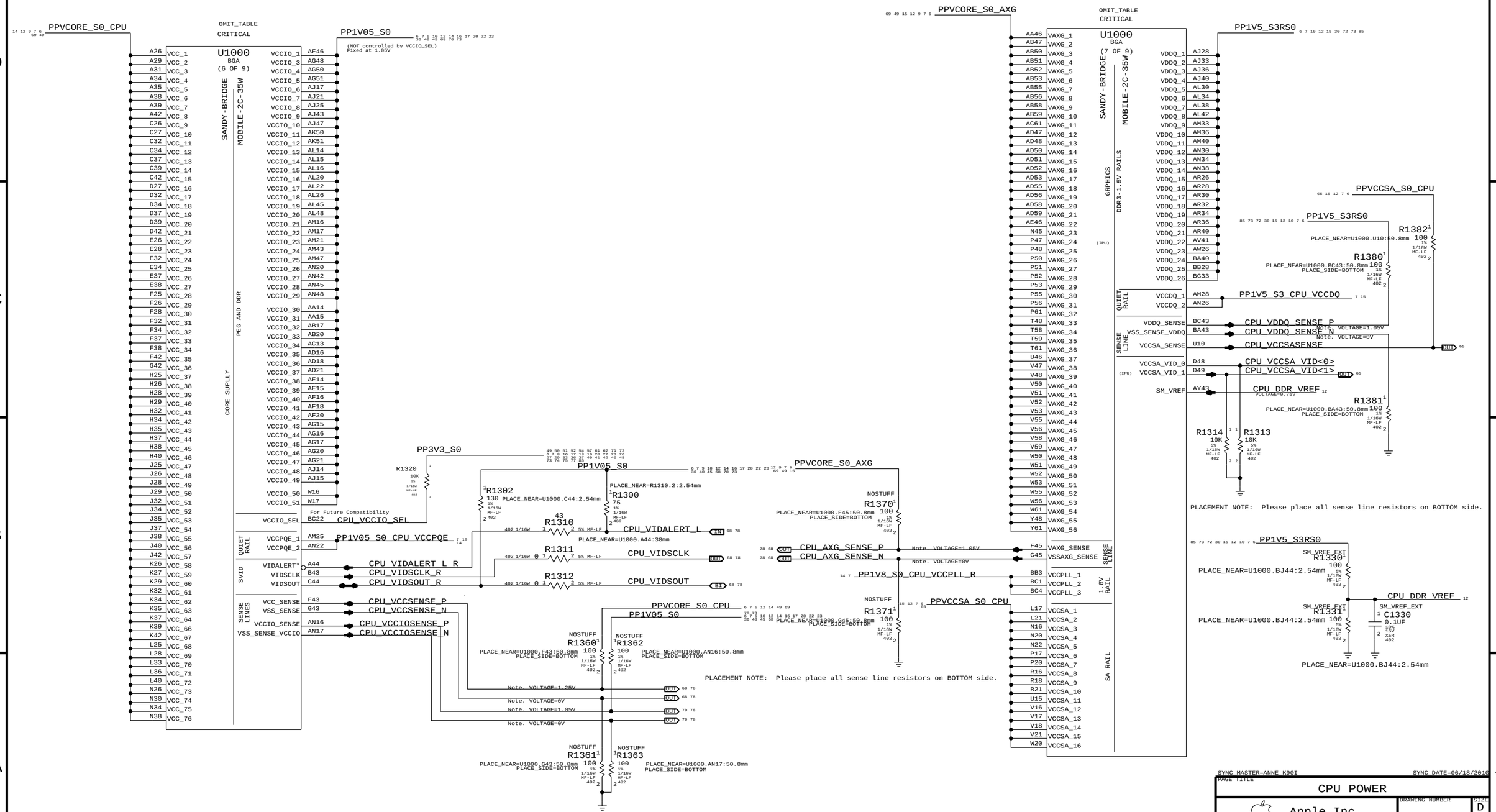

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OMIT_TABLE
CRITICAL

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SANDY-BRIDGE
MOBILE-2C-35W

BG13	VSS	VSS	M11
BG17	VSS	VSS	M15
BG21	VSS	VSS	M58
BG24	VSS	VSS	N1
BG28	VSS	VSS	N17
BG37	VSS	VSS	N21
BG41	VSS	VSS	N25
BG45	VSS	VSS	N28
BG49	VSS	VSS	N33
BG53	VSS	VSS	N36
C29	VSS	VSS	N40
C35	VSS	VSS	N43
C40	VSS	VSS	N47
D4	VSS	VSS	N48
D6	VSS	VSS	N51
D10	VSS	VSS	N52
D14	VSS	VSS	N56
D18	VSS	VSS	N61
D22	VSS	VSS	P9
D26	VSS	VSS	P14
D29	VSS	VSS	P16
D35	VSS	VSS	P18
D40	VSS	VSS	P21
D43	VSS	VSS	P58
D46	VSS	VSS	P59
D50	VSS	VSS	R4
D54	VSS	VSS	R17
D58	VSS	VSS	R20
E3	VSS	VSS	R46
E25	VSS	VSS	T1
E29	VSS	VSS	T47
E35	VSS	VSS	T50
E40	VSS	VSS	T51
F13	VSS	VSS	T52
F15	VSS	VSS	T53
F19	VSS	VSS	T55
F29	VSS	VSS	T56
F35	VSS	VSS	U8
F40	VSS	VSS	U13
F55	VSS	VSS	V20
G6	VSS	VSS	V61
G48	VSS	VSS	W8
G51	VSS	VSS	W13
G61	VSS	VSS	W15
H4	VSS	VSS	W18
H10	VSS	VSS	W21
H14	VSS	VSS	W46
H17	VSS	VSS	Y4
H21	VSS	VSS	Y47
H53	VSS	VSS	Y58
H58	VSS	VSS	Y59
J1	VSS		
J49	VSS		
J55	VSS		
K8	VSS		
K11	VSS		
K21	VSS	VSS_NCTF	A5
K51	VSS	VSS_NCTF	A57
L16	VSS	VSS_NCTF	BC61
L20	VSS	VSS_NCTF	BD3
L22	VSS	VSS_NCTF	BD59
L26	VSS	VSS_NCTF	BE4
L30	VSS	VSS_NCTF	BE58
L34	VSS	VSS_NCTF	BG5
L38	VSS	VSS_NCTF	BG57
L43	VSS	VSS_NCTF	C3
L48	VSS	VSS_NCTF	C58
L61	VSS	VSS_NCTF	D59
M4	VSS	VSS_NCTF	E1
M6	VSS	VSS_NCTF	E61

OMIT_TABLE
CRITICAL

U1000
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SANDY-BRIDGE
MOBILE-2C-35W

A9	VSS	VSS	AM34
A13	VSS	VSS	AM38
A17	VSS	VSS	AM42
A21	VSS	VSS	AM45
A25	VSS	VSS	AM48
A28	VSS	VSS	AM58
A33	VSS	VSS	AN1
A37	VSS	VSS	AN21
A40	VSS	VSS	AN25
A45	VSS	VSS	AN28
A49	VSS	VSS	AN33
A53	VSS	VSS	AN36
AA1	VSS	VSS	AN40
AA8	VSS	VSS	AN43
AA13	VSS	VSS	AN47
AA50	VSS	VSS	AN50
AA51	VSS	VSS	AN54
AA52	VSS	VSS	AP7
AA53	VSS	VSS	AP10
AA55	VSS	VSS	AP51
AA56	VSS	VSS	AP55
AB16	VSS	VSS	AR7
AB18	VSS	VSS	AR13
AB21	VSS	VSS	AR17
AB48	VSS	VSS	AR21
AB61	VSS	VSS	AR41
AC6	VSS	VSS	AR48
AC10	VSS	VSS	AR61
AC14	VSS	VSS	AT4
AC46	VSS	VSS	AT14
AD4	VSS	VSS	AT19
AD17	VSS	VSS	AT36
AD20	VSS	VSS	AT45
AD61	VSS	VSS	AT52
AE8	VSS	VSS	AT58
AE13	VSS	VSS	AU1
AF1	VSS	VSS	AU7
AF17	VSS	VSS	AU11
AF21	VSS	VSS	AU28
AF47	VSS	VSS	AU32
AF48	VSS	VSS	AU51
AF50	VSS	VSS	AV17
AF51	VSS	VSS	AV21
AF52	VSS	VSS	AV22
AF53	VSS	VSS	AV34
AF55	VSS	VSS	AV40
AF56	VSS	VSS	AV48
AF58	VSS	VSS	AV55
AF59	VSS	VSS	AW7
AG7	VSS	VSS	AW13
AG10	VSS	VSS	AW43
AG14	VSS	VSS	AW61
AG18	VSS	VSS	AY4
AG47	VSS	VSS	AY9
AG52	VSS	VSS	AY14
AG61	VSS	VSS	AY19
AH4	VSS	VSS	AY30
AH58	VSS	VSS	AY36
AJ7	VSS	VSS	AY41
AJ13	VSS	VSS	AY45
AJ16	VSS	VSS	AY49
AJ20	VSS	VSS	AY55
AJ22	VSS	VSS	AY58
AJ26	VSS	VSS	BA1
AJ30	VSS	VSS	BA11
AJ34	VSS	VSS	BA17
AJ38	VSS	VSS	BA21
AJ42	VSS	VSS	BA26
AJ45	VSS	VSS	BA32
AJ48	VSS	VSS	BA48
AK1	VSS	VSS	BA51
AK52	VSS	VSS	BB53
AL10	VSS	VSS	BC5
AL13	VSS	VSS	BC13
AL17	VSS	VSS	BC57
AL21	VSS	VSS	BD8
AL25	VSS	VSS	BD12
AL28	VSS	VSS	BD16
AL33	VSS	VSS	BD19
AL36	VSS	VSS	BD23
AL40	VSS	VSS	BD27
AL43	VSS	VSS	BD32
AL47	VSS	VSS	BD36
AL61	VSS	VSS	BD40
AM4	VSS	VSS	BD44
AM13	VSS	VSS	BD48
AM20	VSS	VSS	BD52
AM22	VSS	VSS	BD56
AM26	VSS	VSS	BE5
AM30	VSS	VSS	BG9

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All INTEL recommendations from Intel doc #4439028 Huron River Platform Power Design Guide

CPU VCORE DECOUPLING

Intel recommendation (Section 6.2): 35x 2.2uF, 25x 22uF, 4x 470uF

69 49 12 9 7 6 PPVCORE_S0_CPU

C1600 2.2UF 20% 4V X5R 402 CRITICAL
C1601 2.2UF 20% 4V X5R 402 NOSTUFF
C1602 2.2UF 20% 4V X5R 402 NOSTUFF
C1603 2.2UF 20% 4V X5R 402 CRITICAL
C1604 2.2UF 20% 4V X5R 402 CRITICAL
C1605 2.2UF 20% 4V X5R 402 NOSTUFF
C1606 2.2UF 20% 4V X5R 402 CRITICAL
C1607 2.2UF 20% 4V X5R 402 CRITICAL
C1608 2.2UF 20% 4V X5R 402 CRITICAL
C1609 2.2UF 20% 4V X5R 402 CRITICAL
C1610 2.2UF 20% 4V X5R 402 CRITICAL
C1611 2.2UF 20% 4V X5R 402 NOSTUFF
C1612 2.2UF 20% 4V X5R 402 CRITICAL
C1613 2.2UF 20% 4V X5R 402 CRITICAL
C1614 2.2UF 20% 4V X5R 402 NOSTUFF
C1615 2.2UF 20% 4V X5R 402 CRITICAL
C1616 2.2UF 20% 4V X5R 402 NOSTUFF
C1617 2.2UF 20% 4V X5R 402 CRITICAL
C1618 2.2UF 20% 4V X5R 402 NOSTUFF
C1619 2.2UF 20% 4V X5R 402 NOSTUFF
C1620 2.2UF 20% 4V X5R 402 NOSTUFF
C1621 2.2UF 20% 4V X5R 402 NOSTUFF
C1622 2.2UF 20% 4V X5R 402 NOSTUFF
C1623 2.2UF 20% 4V X5R 402 CRITICAL
C1624 2.2UF 20% 4V X5R 402 CRITICAL

C1625 2.2UF 20% 4V X5R 402 CRITICAL
C1626 2.2UF 20% 4V X5R 402 NOSTUFF
C1627 2.2UF 20% 4V X5R 402 CRITICAL
C1628 2.2UF 20% 4V X5R 402 CRITICAL
C1629 2.2UF 20% 4V X5R 402 NOSTUFF
C1630 2.2UF 20% 4V X5R 402 NOSTUFF
C1631 2.2UF 20% 4V X5R 402 CRITICAL
C1632 2.2UF 20% 4V X5R 402 CRITICAL
C1633 2.2UF 20% 4V X5R 402 NOSTUFF
C1634 2.2UF 20% 4V X5R 402 NOSTUFF
C1635 2.2UF 20% 4V X5R 402 CRITICAL
C1636 2.2UF 20% 4V X5R 402 NOSTUFF
C1637 2.2UF 20% 4V X5R 402 CRITICAL
C1638 2.2UF 20% 4V X5R 402 CRITICAL
C1639 2.2UF 20% 4V X5R 402 NOSTUFF
C1640 2.2UF 20% 4V X5R 402 CRITICAL
C1641 2.2UF 20% 4V X5R 402 CRITICAL
C1642 2.2UF 20% 4V X5R 402 CRITICAL
C1643 2.2UF 20% 4V X5R 402 CRITICAL
C1644 2.2UF 20% 4V X5R 402 CRITICAL
C1645 2.2UF 20% 4V X5R 402 CRITICAL
C1646 2.2UF 20% 4V X5R 402 NOSTUFF
C1647 2.2UF 20% 4V X5R 402 CRITICAL
C1648 2.2UF 20% 4V X5R 402 CRITICAL
C1649 2.2UF 20% 4V X5R 402 NOSTUFF

C1650 2.2UF 20% 4V X5R 402 CRITICAL
C1651 2.2UF 20% 4V X5R 402 CRITICAL
C1652 2.2UF 20% 4V X5R 402 CRITICAL
C1653 2.2UF 20% 4V X5R 402 CRITICAL
C1654 2.2UF 20% 4V X5R 402 CRITICAL

PLACEMENT_NOTE (C1655-C1666):
Place close to U1000 on top side.

C1655 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1656 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL NOSTUFF
C1657 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL NOSTUFF
C1658 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL NOSTUFF
C1659 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL NOSTUFF
C1660 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1661 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1662 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1663 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1664 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1665 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1666 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	16	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG		CRITICAL	
		C1655,C1660,C1661,C1662,C1663,C1664,C1665,C1666,C1667,C1670,C1671,C1674,C1676,C1677,C1678,C1679			

PLACEMENT_NOTE (C1667-C1679):
Place close to U1000 on bottom side.

C1667 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1668 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL NOSTUFF
C1669 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL NOSTUFF
C1670 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1671 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1672 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL NOSTUFF
C1673 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL NOSTUFF
C1674 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1675 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL NOSTUFF
C1676 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1677 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1678 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT
C1679 22UF 20% 6.3V X5R-CERM-1 603 CRITICAL OMIT

PLACEMENT_NOTE (C1640-C1645):
Place near inductors on bottom side.

C1680 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1681 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1682 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1683 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

CPU VCCIO/VCCPQ DECOUPLING

Intel recommendation (Section 6.5): 26x 1uF, 10x 10uF, 2x 330uF

PLACEMENT_NOTE (C1684-C167F):
Place on bottom side of U1000

45 40 36 23 12 10 8 5 PP1V05_S0
22 20 17 16 73 70 68

C1684 1UF 10% 10V X5R 402
C1685 1UF 10% 10V X5R 402
C1686 1UF 10% 10V X5R 402
C1687 1UF 10% 10V X5R 402
C1688 1UF 10% 10V X5R 402
C1689 1UF 10% 10V X5R 402
C1690 1UF 10% 10V X5R 402
C1691 1UF 10% 10V X5R 402
C1692 1UF 10% 10V X5R 402
C1693 1UF 10% 10V X5R 402
C1694 1UF 10% 10V X5R 402
C1695 1UF 10% 10V X5R 402
C1696 1UF 10% 10V X5R 402

C1697 1UF 10% 10V X5R 402
C1698 1UF 10% 10V X5R 402
C1699 1UF 10% 10V X5R 402
C169A 1UF 10% 10V X5R 402
C169B 1UF 10% 10V X5R 402
C169C 1UF 10% 10V X5R 402
C169D 1UF 10% 10V X5R 402
C169E 1UF 10% 10V X5R 402
C169F 1UF 10% 10V X5R 402
C161A 1UF 10% 10V X5R 402
C161B 1UF 10% 10V X5R 402
C161C 1UF 10% 10V X5R 402
C161D 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1672-C1681):
Place near U1000 on bottom side

C161E 10UF 20% 6.3V X5R 603
C161F 10UF 20% 6.3V CERM-X5R 0402-1
C162A 10UF 20% 6.3V CERM-X5R 0402-1
C162B 10UF 20% 6.3V CERM-X5R 0402-1
C162C 10UF 20% 6.3V CERM-X5R 0402-1
C162D 10UF 20% 6.3V CERM-X5R 0402-1
C162E 10UF 20% 6.3V CERM-X5R 0402-1
C167A 10UF 20% 6.3V CERM-X5R 0402-1
C167B 10UF 20% 6.3V CERM-X5R 0402-1
C167C 10UF 20% 6.3V CERM-X5R 0402-1

C167D 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
C167E 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhm resistor, 1x 1uF 0402

R1601 0.010 1% 1/4W MF 0603
PP1V05_S0_CPU_VCCPQE 7 10 12
C167F 1UF 10% 10V X5R 402

Note:The smallest 10mOhm available in the library are 0805s

CPU VCCPLL DECOUPLING

Intel recommendation (section 6.4): 2x 1uF, 1x 330uF

PLACEMENT_NOTE (C1646-C1671):
Place near U1000 on top side

71 26 22 20 17 7 6 PP1VR_S0
R1600 0 5% 1/16W MF-LF 402
PP1VR_S0_CPU_VCCPLL_R 7 12
PLACE_NEAR=U1000.AK61:5mm
PLACE_NEAR=U1000.AK63:2.54 mm:NO_VIA
C160X 1UF 10% 10V X5R 402
C160Y 1UF 10% 10V X5R 402
C160Z 330UF-0.006OHM 20% 2V POLY CASE-D2-SM
PLACE_NEAR=U1000.AK65:2.54 mm:NO_VIA

CPU VCCPLL Low pass filter

SYNC_MASTER=JACK_K90I SYNC_DATE=06/28/2010

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VAXG DECOUPLING

Intel recommendation (section 6.3): 21x 1uF, 6x 10uF, 6x 22uF, 2x 470uF

69 49 12 9 7 6 PPVCORE_S0_AXG

PLACEMENT_NOTE (C1700-C1710):

Place on bottom side of U1000

CRITICAL C1700 1UF 10% 10V X5R 402
CRITICAL C1701 1UF 10% 10V X5R 402
CRITICAL C1702 1UF 10% 10V X5R 402
CRITICAL C1703 1UF 10% 10V X5R 402
CRITICAL C1704 1UF 10% 10V X5R 402
CRITICAL C1705 1UF 10% 10V X5R 402
CRITICAL C1706 1UF 10% 10V X5R 402
CRITICAL C1707 1UF 10% 10V X5R 402
CRITICAL C1708 1UF 10% 10V X5R 402
CRITICAL C1709 1UF 10% 10V X5R 402
CRITICAL C1710 1UF 10% 10V X5R 402

PLACEMENT_NOTE (C1711-C1716):

CRITICAL C1711 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1712 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1713 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1714 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1715 10UF 20% 6.3V CERM-X5R 0402-1
CRITICAL C1716 10UF 20% 6.3V CERM-X5R 0402-1

PLACEMENT_NOTE (C1717-C1722):

CRITICAL OMIT C1717 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1718 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1719 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1720 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1721 22UF 20% 6.3V X5R-CERM-1 603
CRITICAL OMIT C1722 22UF 20% 6.3V X5R-CERM-1 603

PLACEMENT_NOTE (C1723-C1724):

Place near inductors on bottom side.

C1723 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM
C1724 470UF-4MOHM 20% 2.0V POLY-TANT D2T-SM

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
138S0691	6	CAP,CER,X5R,22uF,20%,6.3V,0603,SAMSUNG	C1717,C1718,C1719,C1720,C1721,C1722	CRITICAL	

CPU VDDQ/VCCDQ DECOUPLING

Intel recommendation (Section 6.5): 10x 1uF, 8x 10uF, 1x 330uF

PLACEMENT_NOTE (C1738-C1747):

85 73 72 30 12 10 7 6 PP1V5_S3RS0

Place on bottom side of U1000

C1738 1UF 10% 10V X5R 402
C1739 1UF 10% 10V X5R 402
C1740 1UF 10% 10V X5R 402
C1741 1UF 10% 10V X5R 402
C1742 1UF 10% 10V X5R 402
C1743 1UF 10% 10V X5R 402
C1744 1UF 10% 10V X5R 402
C1745 1UF 10% 10V X5R 402
C1746 1UF 10% 10V X5R 402
C1747 1UF 10% 10V X5R 402

Place close to U1000 on bottom side

C1748 10UF 20% 6.3V CERM-X5R 0402-1
C1749 10UF 20% 6.3V CERM-X5R 0402-1
C1750 10UF 20% 6.3V X5R 603
C1751 10UF 20% 6.3V CERM-X5R 0402-1
C1752 10UF 20% 6.3V CERM-X5R 0402-1
C1753 10UF 20% 6.3V CERM-X5R 0402-1
C1754 10UF 20% 6.3V X5R 603
C1755 10UF 20% 6.3V CERM-X5R 0402-1

C1756 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

Intel recommendation: 1x 10mOhn resistor, 1x 1uF 0402

R1702 0.010 1% 1/4W MF 0603

PP1V5_S3_CPU_VCCDQ 7 12

C1757 1UF 10% 10V X5R 402

CPU VCCSA DECOUPLING

Intel recommendation (Section 6.6): 6x 1uf, 5x 10uf, 1x 330uf

PLACEMENT_NOTE (C1758-C1762):

65 12 7 6 PPVCCSA_S0_CPU

Place on bottom side of U1000

C1758 1UF 10% 10V X5R 402
C1759 1UF 10% 10V X5R 402
C1760 1UF 10% 10V X5R 402
C1761 1UF 10% 10V X5R 402
C1762 1UF 10% 10V X5R 402

C1763 10UF 20% 6.3V CERM-X5R 0402-1
C1764 10UF 20% 6.3V CERM-X5R 0402-1
C1765 10UF 20% 6.3V CERM-X5R 0402-1
C1766 10UF 20% 6.3V CERM-X5R 0402-1
C1767 10UF 20% 6.3V CERM-X5R 0402-1

C1768 330UF-0.006OHM 20% 2V POLY CASE-D2-SM

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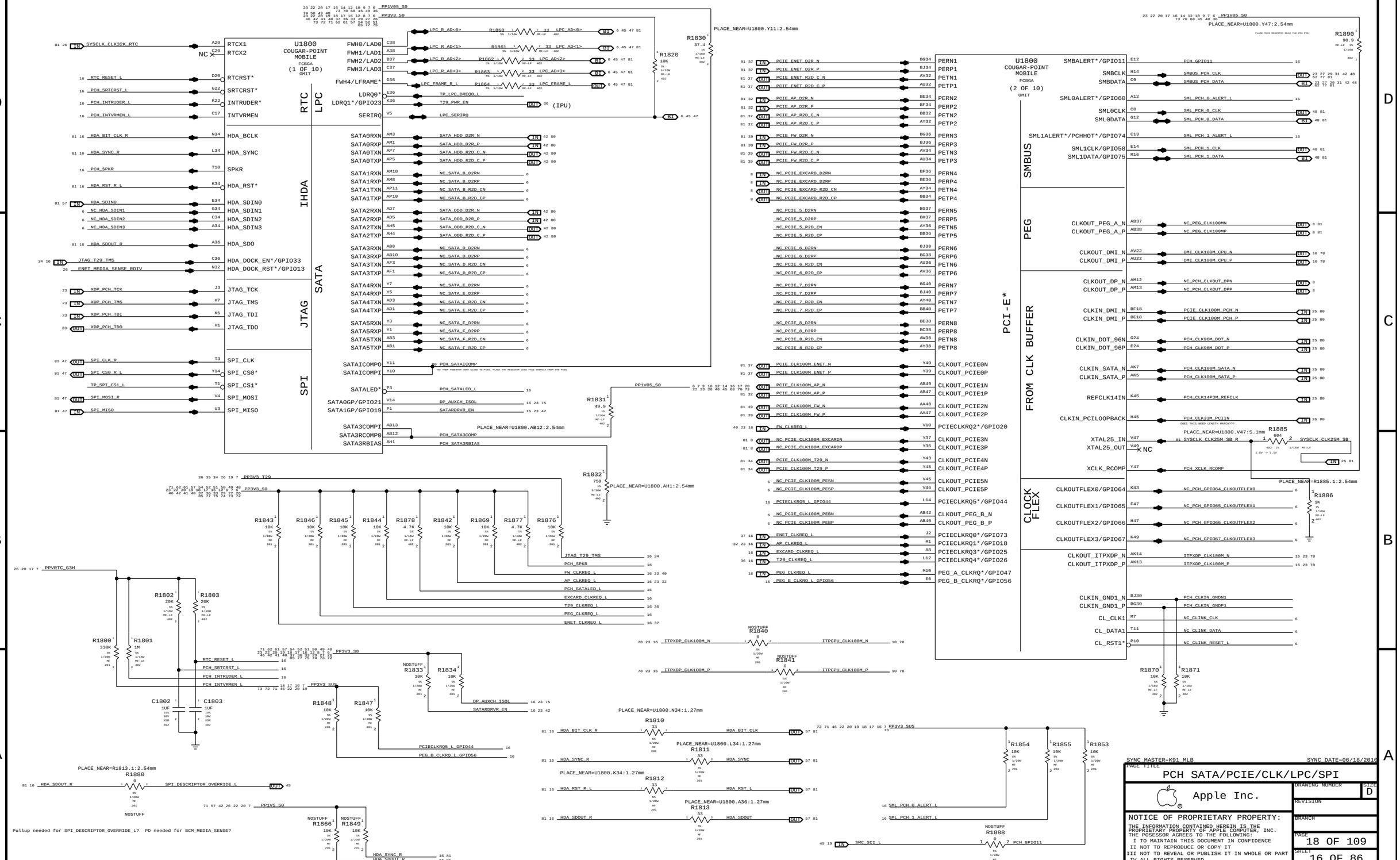

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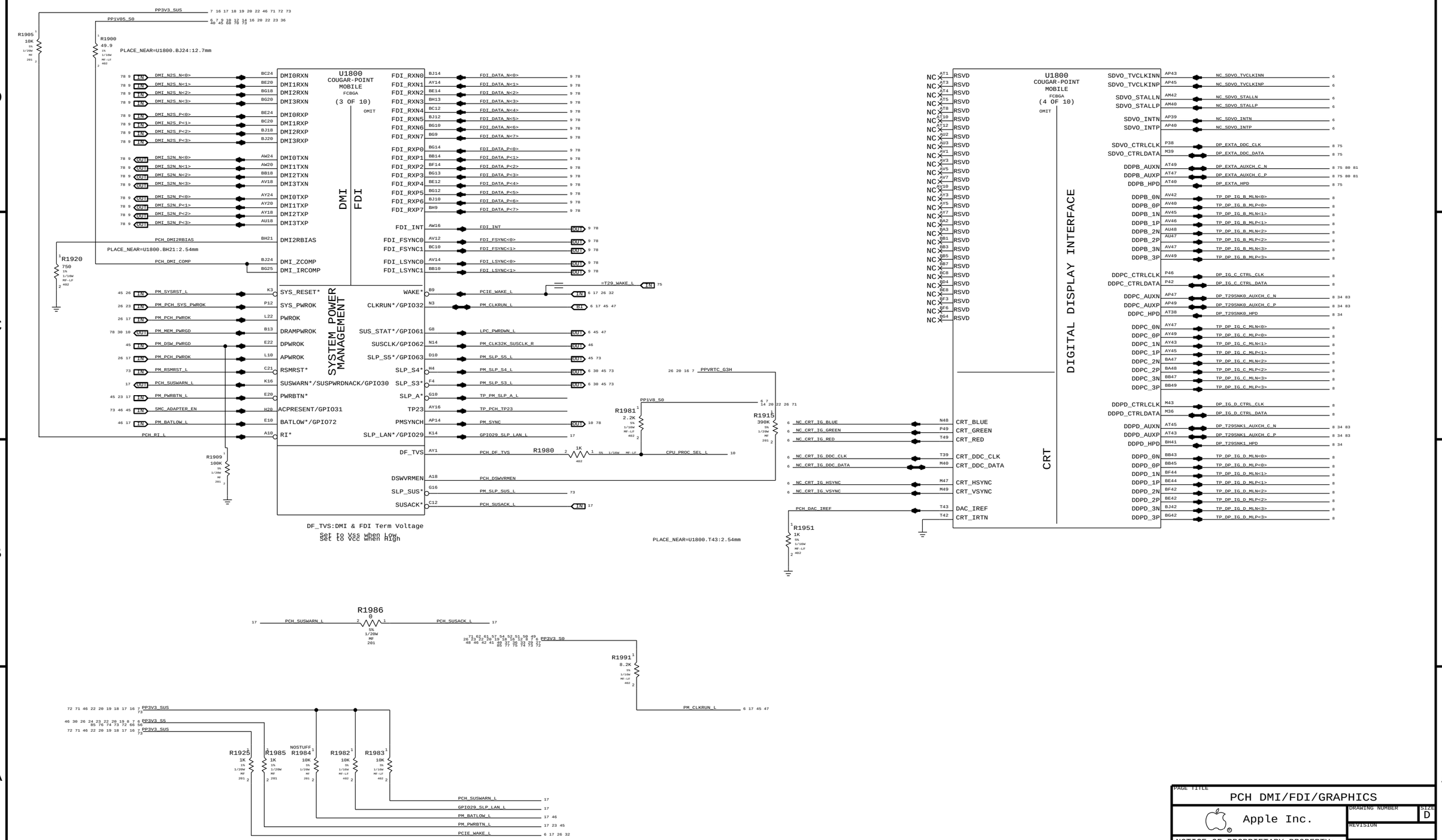

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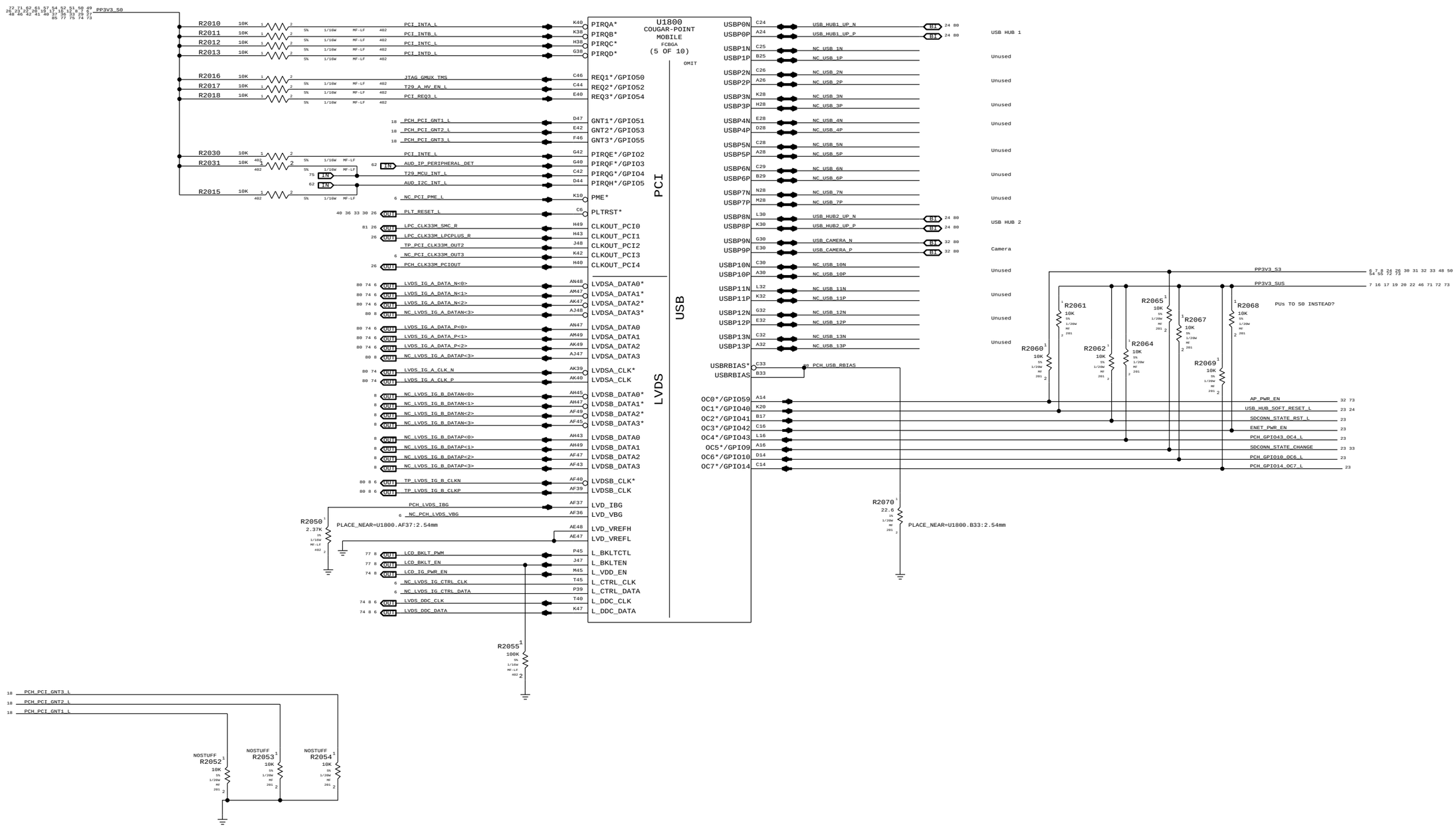

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PAGE TITLE: PCH PCI/FLASHCACHE/USB

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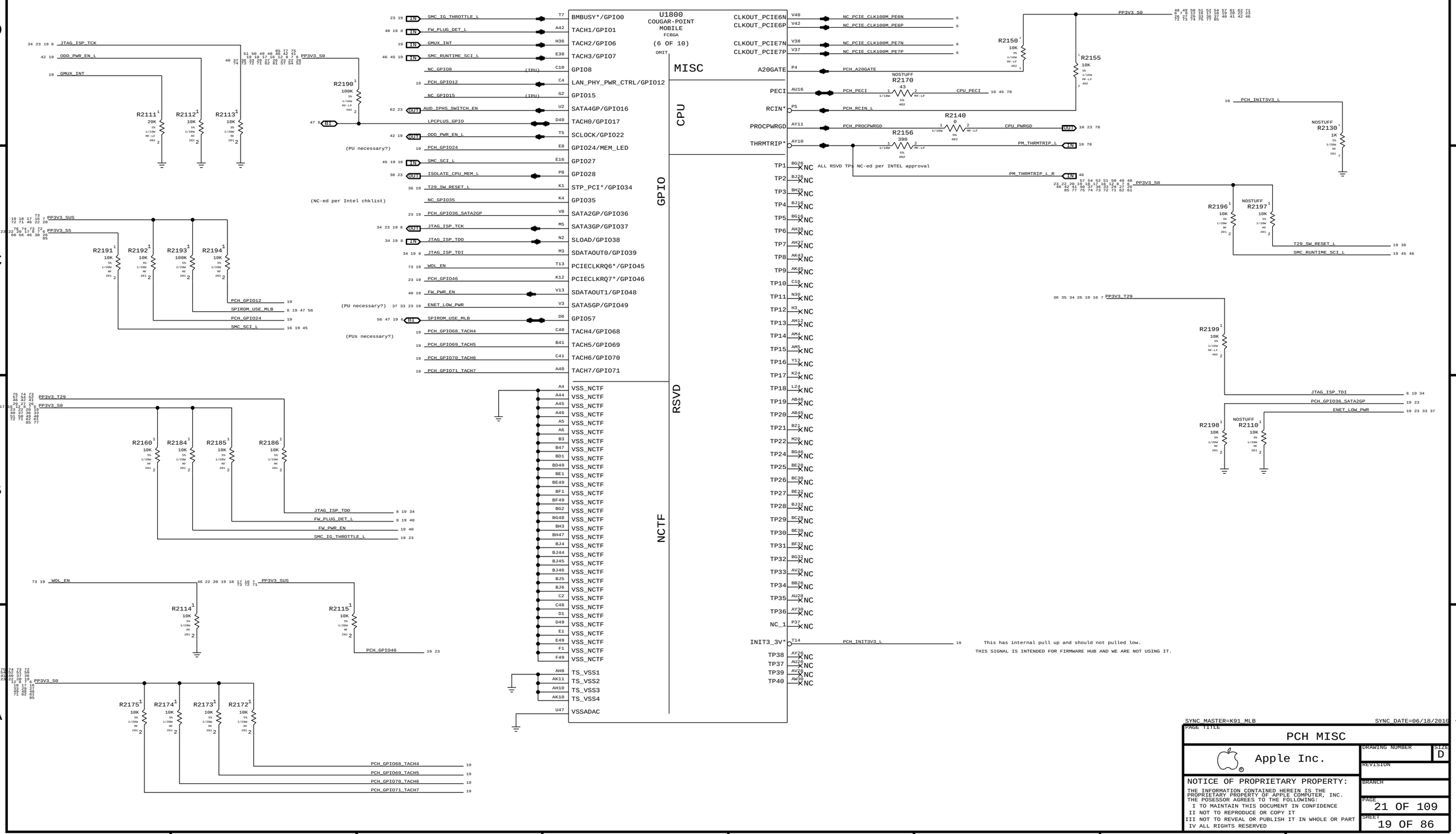

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PAGE TITLE

PCH MISC

Apple Inc.

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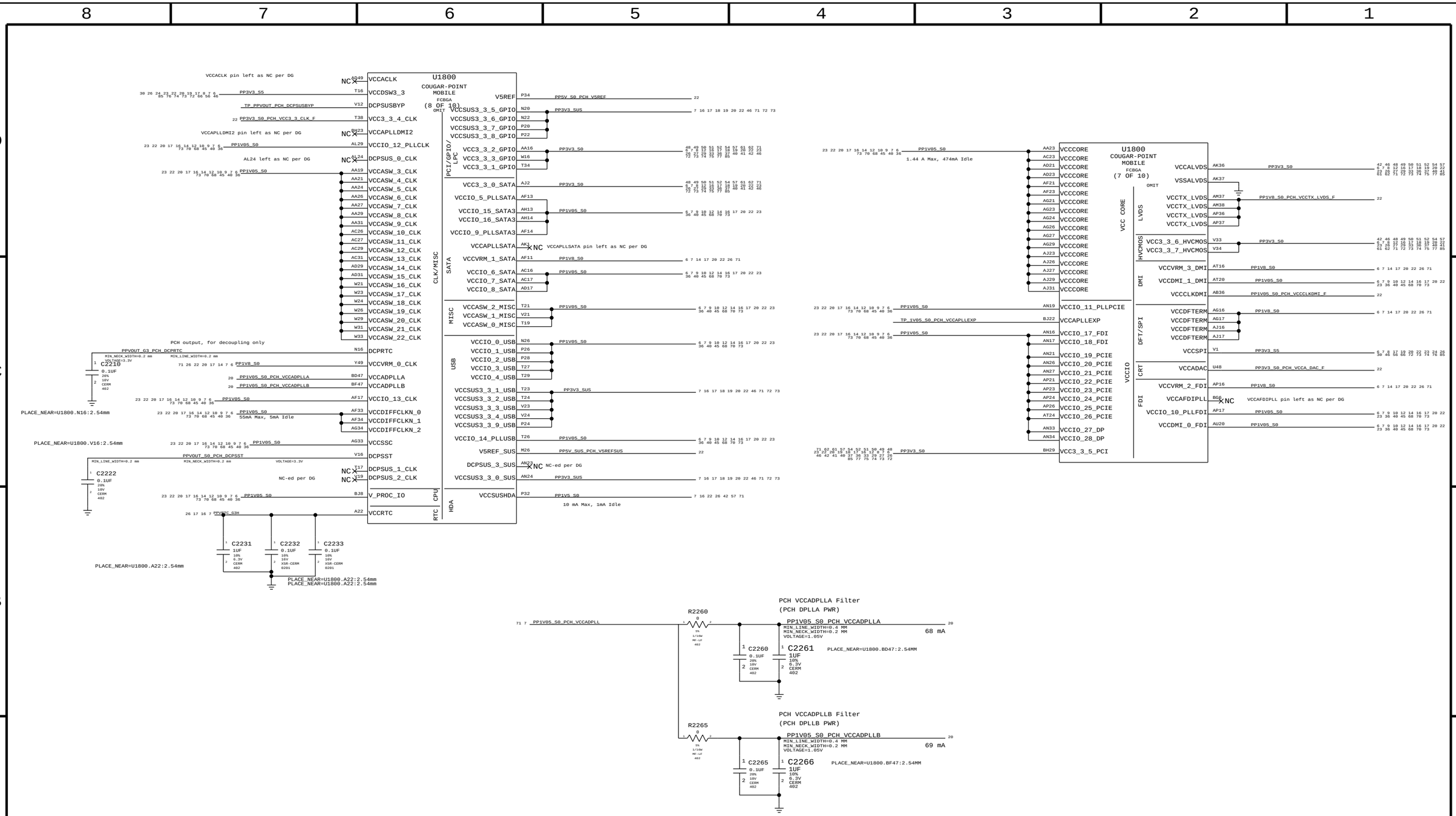

PAGE TITLE
PCH POWER

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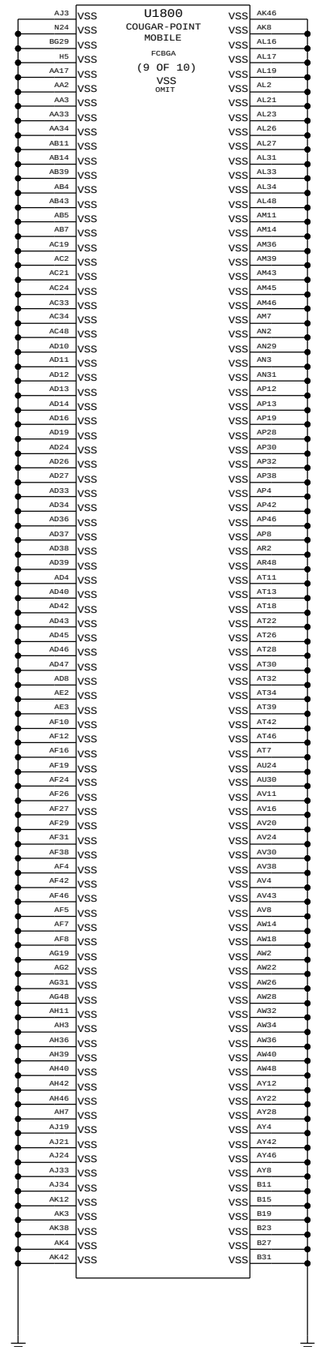

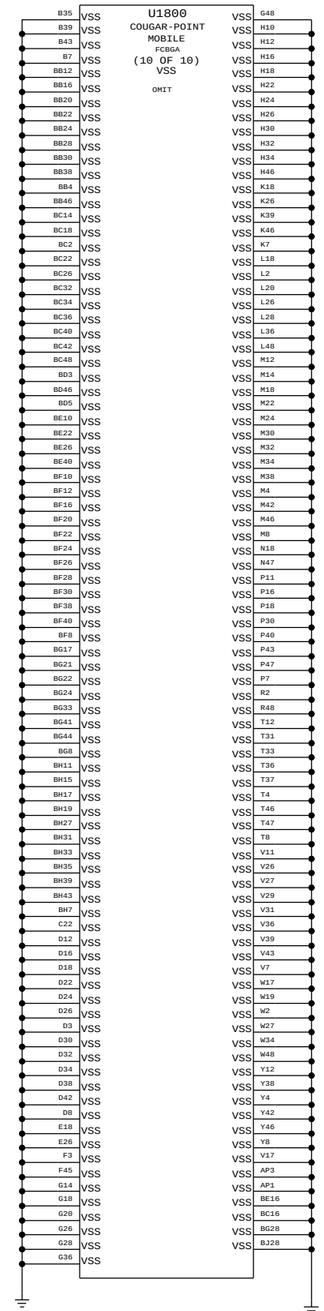

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PAGE TITLE

PCH GROUNDS

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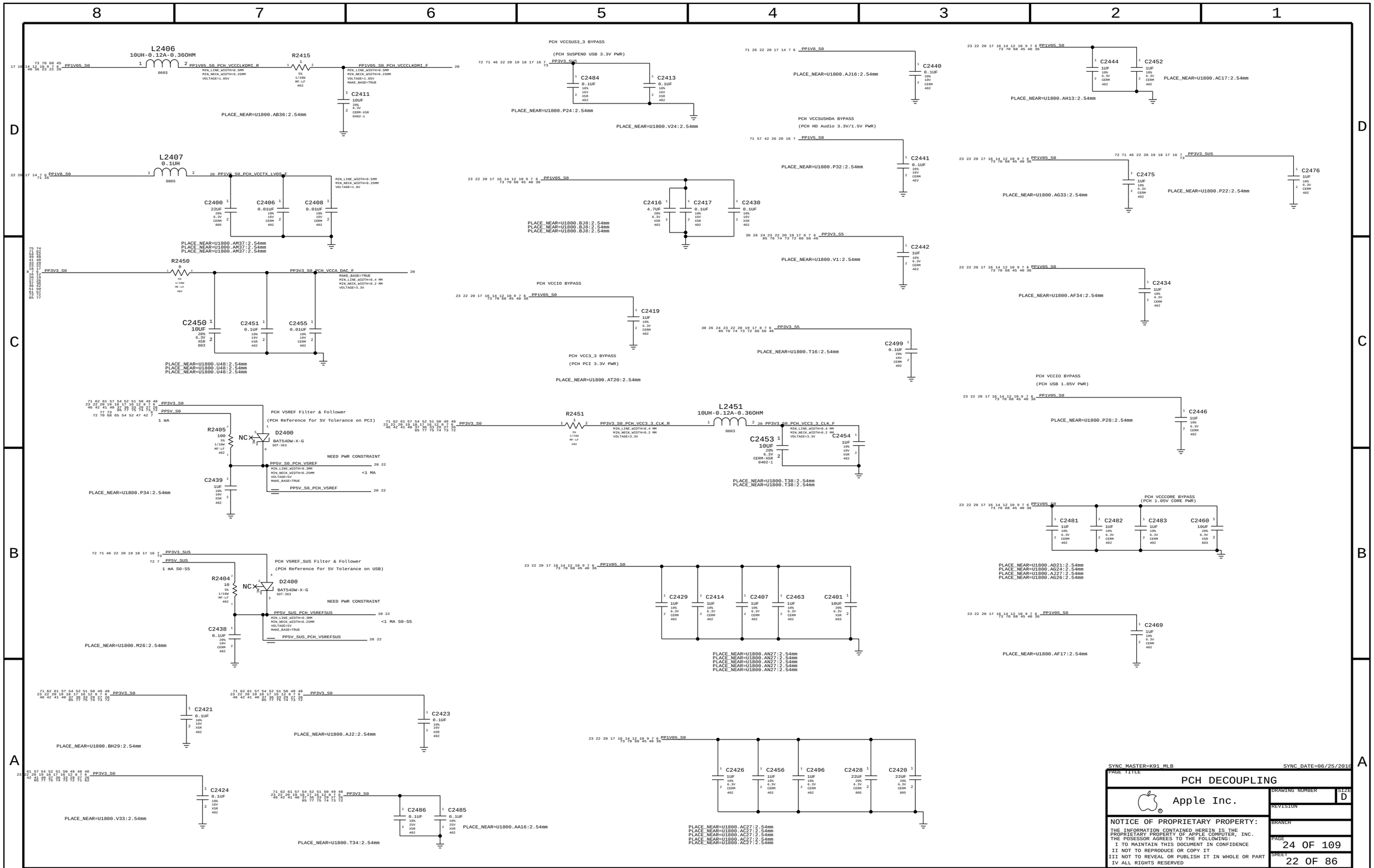

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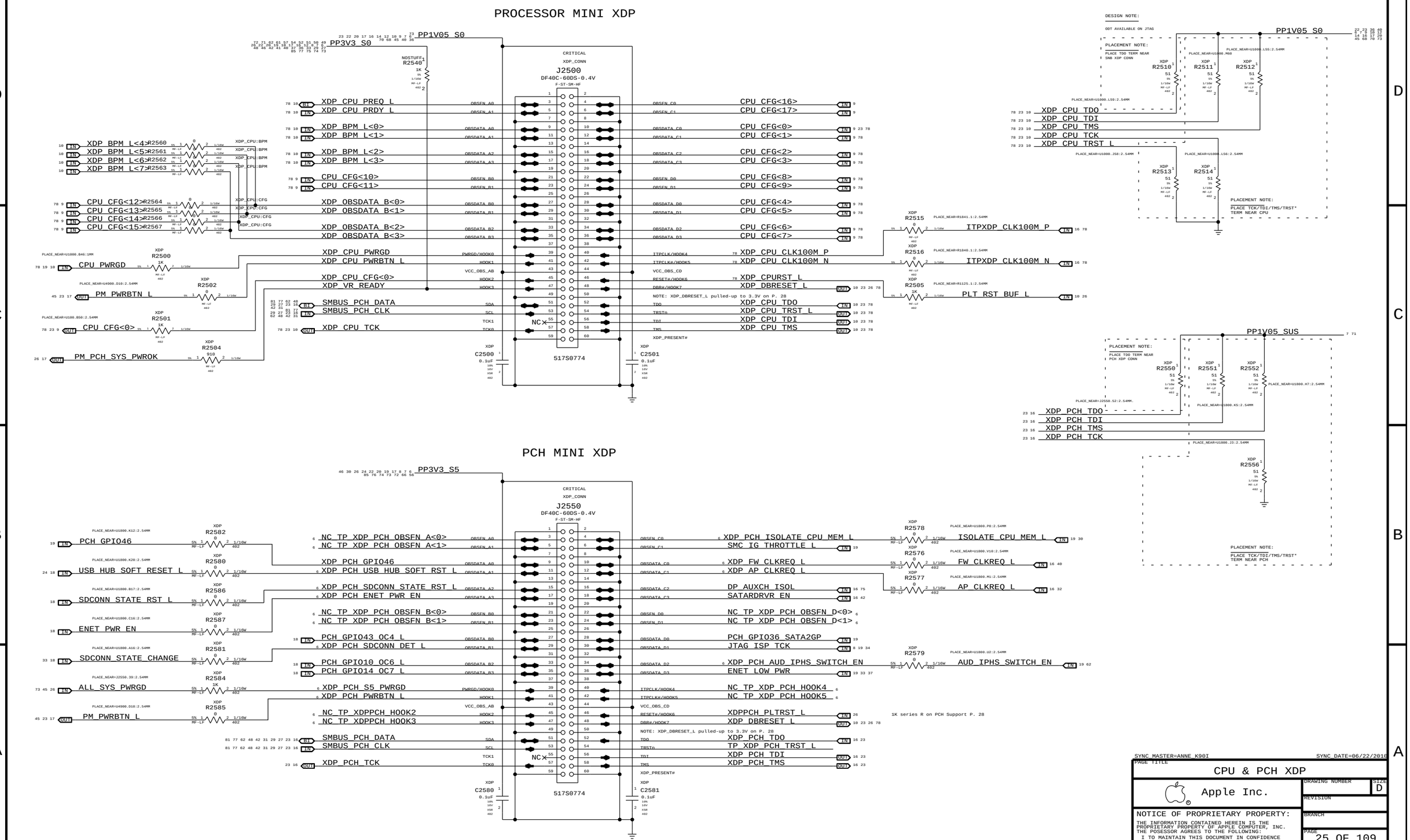

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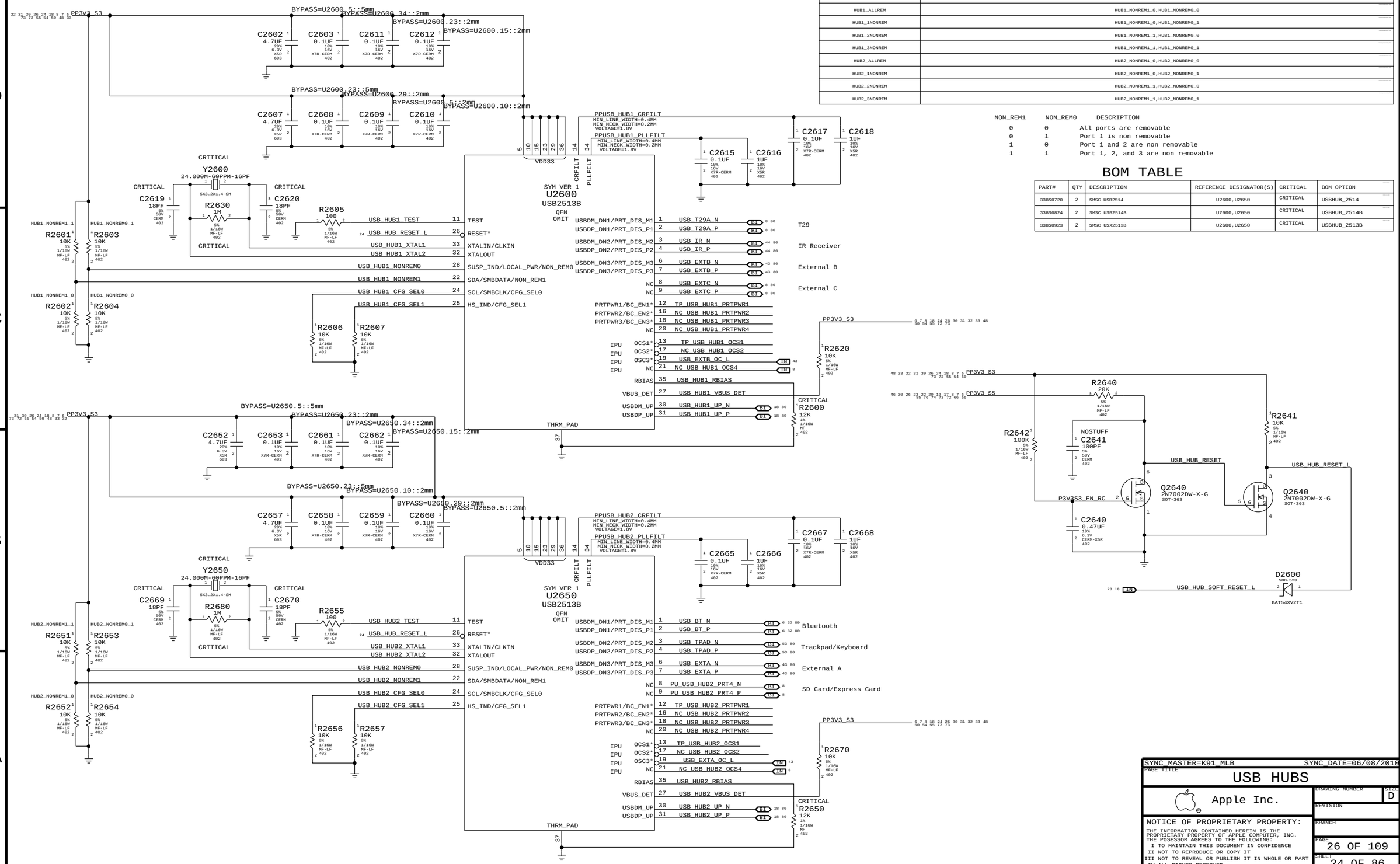

BOM GROUP	BOM OPTIONS
HUB1_ALLREM	HUB1_NONREM1_0,HUB1_NONREM0_0
HUB1_1NONREM	HUB1_NONREM1_0,HUB1_NONREM0_1
HUB1_2NONREM	HUB1_NONREM1_1,HUB1_NONREM0_0
HUB1_3NONREM	HUB1_NONREM1_1,HUB1_NONREM0_1
HUB2_ALLREM	HUB2_NONREM1_0,HUB2_NONREM0_0
HUB2_1NONREM	HUB2_NONREM1_0,HUB2_NONREM0_1
HUB2_2NONREM	HUB2_NONREM1_1,HUB2_NONREM0_0
HUB2_3NONREM	HUB2_NONREM1_1,HUB2_NONREM0_1

NON_REM1	NON_REM0	DESCRIPTION
0	0	All ports are removable
0	1	Port 1 is non removable
1	0	Port 1 and 2 are non removable
1	1	Port 1, 2, and 3 are non removable

BOM TABLE

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
338S0720	2	SMSC USB2514	U2600,U2650	CRITICAL	USBHUB_2514
338S0824	2	SMSC USB2514B	U2600,U2650	CRITICAL	USBHUB_2514B
338S0923	2	SMSC USX2513B	U2600,U2650	CRITICAL	USBHUB_2513B

SYNC MASTER=K91_MLB SYNC DATE=06/08/2010

PAGE TITLE

USB HUBS

Apple Inc.

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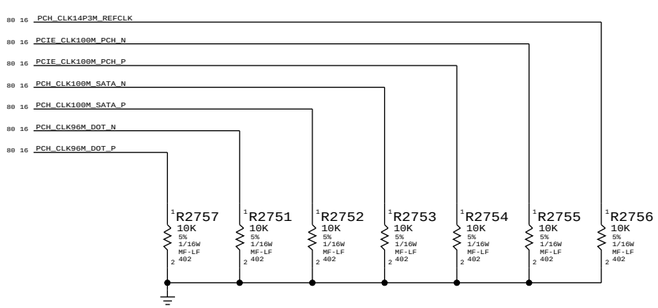
UNUSED clock terminations for FCIM MODE



SYNC_MASTER=K91_MLB SYNC_DATE=06/21/2010

PAGE TITLE

Clock (CK505)

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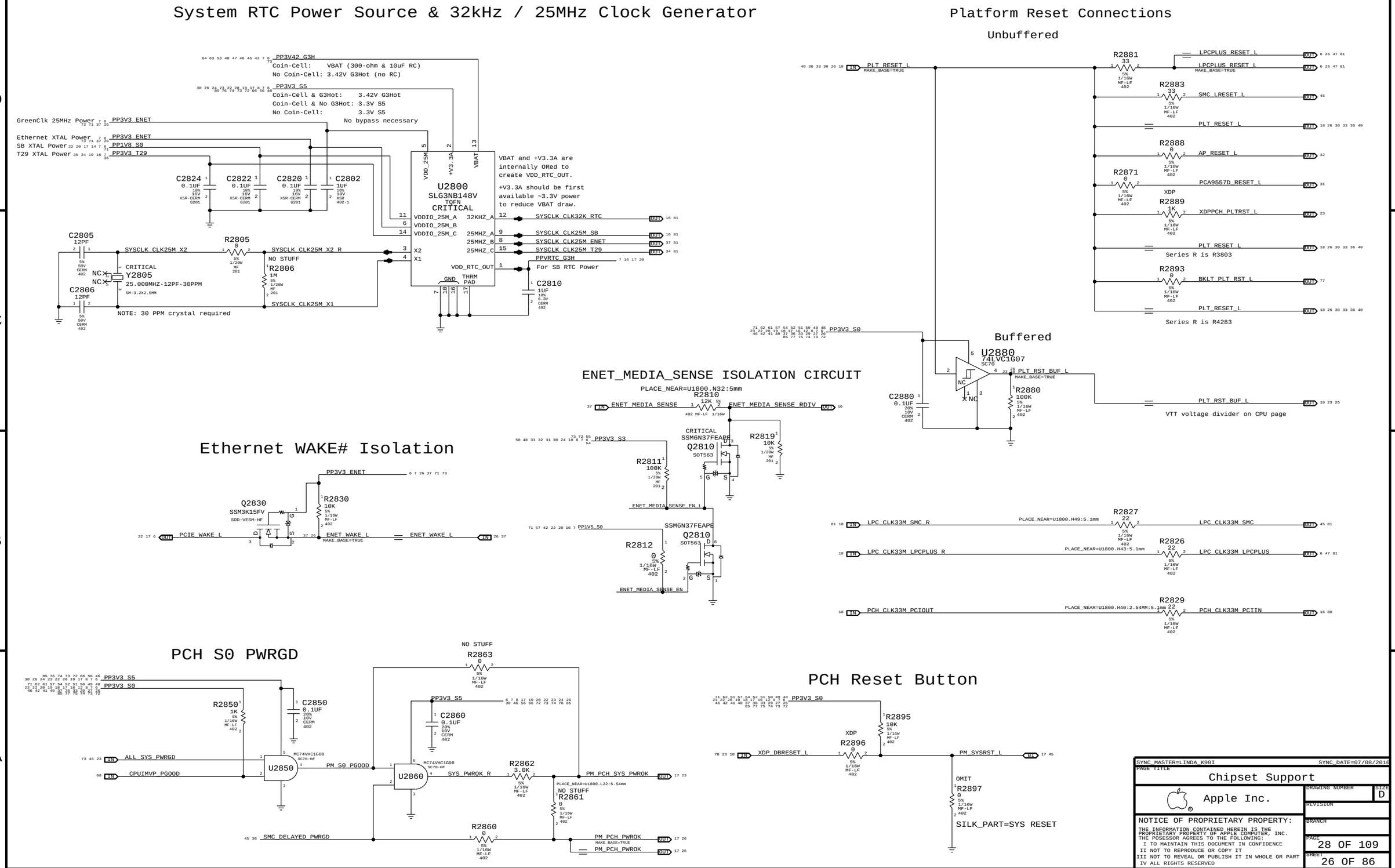

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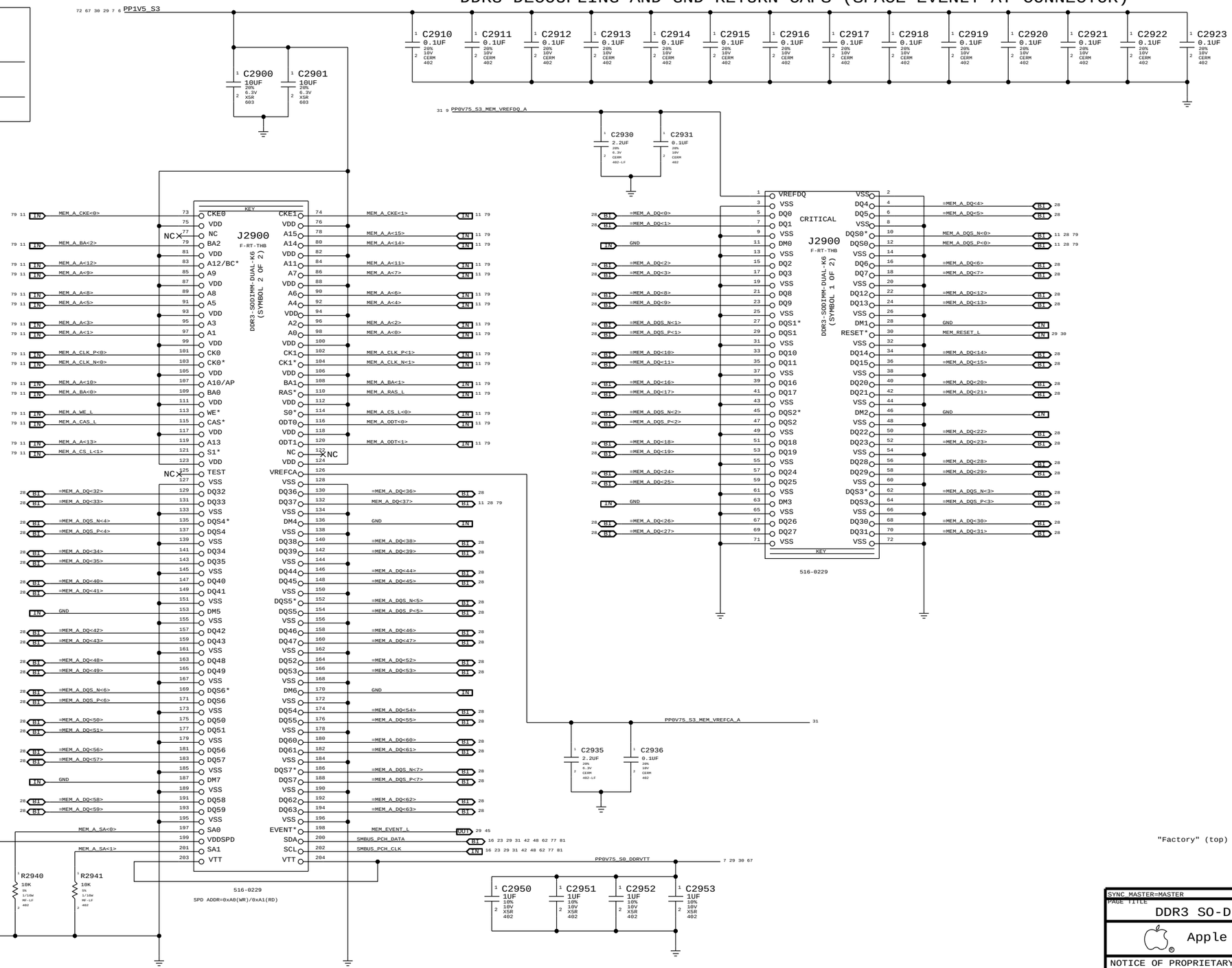
Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_A
- =PP1V5_S3_MEM_A
- =PP0V75_S0_MEM_VTT_A
- =PP5PO_S0_MEM_A (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMA_SCL
- =I2C_SODIMMA_SDA

BOM options provided by this page:
(NONE)

DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)



"Factory" (top) slot

SYNC_MASTER=MASTER SYNC_DATE=MASTER

PAGE TITLE
DDR3 SO-DIMM Connector A

Apple Inc.

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CPU CHANNEL A DQS 0 -> DIMM A DQS 0		CPU CHANNEL B DQS 0 -> DIMM B DQS 0	
MEM_A_DQS_N<0>	MEM_A_DQS_N<0>	MEM_B_DQS_N<0>	MEM_B_DQS_N<0>
MEM_A_DQS_P<0>	MEM_A_DQS_P<0>	MEM_B_DQS_P<0>	MEM_B_DQS_P<0>
	GND		GND
MEM_A_DQ<7>	=MEM_A_DQ<3>	MEM_B_DQ<7>	=MEM_B_DQ<3>
MEM_A_DQ<6>	=MEM_A_DQ<6>	MEM_B_DQ<6>	=MEM_B_DQ<2>
MEM_A_DQ<5>	=MEM_A_DQ<1>	MEM_B_DQ<5>	=MEM_B_DQ<0>
MEM_A_DQ<4>	=MEM_A_DQ<5>	MEM_B_DQ<4>	=MEM_B_DQ<4>
MEM_A_DQ<3>	=MEM_A_DQ<2>	MEM_B_DQ<3>	=MEM_B_DQ<7>
MEM_A_DQ<2>	=MEM_A_DQ<7>	MEM_B_DQ<2>	=MEM_B_DQ<6>
MEM_A_DQ<1>	=MEM_A_DQ<0>	MEM_B_DQ<1>	=MEM_B_DQ<5>
MEM_A_DQ<0>	=MEM_A_DQ<4>	MEM_B_DQ<0>	=MEM_B_DQ<1>
CPU CHANNEL A DQS 1 -> DIMM A DQS 1		CPU CHANNEL B DQS 1 -> DIMM B DQS 1	
MEM_A_DQS_N<1>	=MEM_A_DQS_N<1>	MEM_B_DQS_N<1>	=MEM_B_DQS_N<1>
MEM_A_DQS_P<1>	=MEM_A_DQS_P<1>	MEM_B_DQS_P<1>	=MEM_B_DQS_P<1>
	GND		GND
MEM_A_DQ<15>	=MEM_A_DQ<11>	MEM_B_DQ<15>	=MEM_B_DQ<15>
MEM_A_DQ<14>	=MEM_A_DQ<10>	MEM_B_DQ<14>	=MEM_B_DQ<14>
MEM_A_DQ<13>	=MEM_A_DQ<12>	MEM_B_DQ<13>	=MEM_B_DQ<13>
MEM_A_DQ<12>	=MEM_A_DQ<9>	MEM_B_DQ<12>	=MEM_B_DQ<8>
MEM_A_DQ<11>	=MEM_A_DQ<15>	MEM_B_DQ<11>	=MEM_B_DQ<11>
MEM_A_DQ<10>	=MEM_A_DQ<14>	MEM_B_DQ<10>	=MEM_B_DQ<10>
MEM_A_DQ<9>	=MEM_A_DQ<13>	MEM_B_DQ<9>	=MEM_B_DQ<12>
MEM_A_DQ<8>	=MEM_A_DQ<8>	MEM_B_DQ<8>	=MEM_B_DQ<9>
CPU CHANNEL A DQS 2 -> DIMM A DQS 2		CPU CHANNEL B DQS 2 -> DIMM B DQS 2	
MEM_A_DQS_N<2>	=MEM_A_DQS_N<2>	MEM_B_DQS_N<2>	=MEM_B_DQS_N<2>
MEM_A_DQS_P<2>	=MEM_A_DQS_P<2>	MEM_B_DQS_P<2>	=MEM_B_DQS_P<2>
	GND		GND
MEM_A_DQ<23>	=MEM_A_DQ<23>	MEM_B_DQ<23>	=MEM_B_DQ<23>
MEM_A_DQ<22>	=MEM_A_DQ<22>	MEM_B_DQ<22>	=MEM_B_DQ<18>
MEM_A_DQ<21>	=MEM_A_DQ<21>	MEM_B_DQ<21>	=MEM_B_DQ<16>
MEM_A_DQ<20>	=MEM_A_DQ<20>	MEM_B_DQ<20>	=MEM_B_DQ<17>
MEM_A_DQ<19>	=MEM_A_DQ<18>	MEM_B_DQ<19>	=MEM_B_DQ<22>
MEM_A_DQ<18>	=MEM_A_DQ<19>	MEM_B_DQ<18>	=MEM_B_DQ<19>
MEM_A_DQ<17>	=MEM_A_DQ<16>	MEM_B_DQ<17>	=MEM_B_DQ<21>
MEM_A_DQ<16>	=MEM_A_DQ<17>	MEM_B_DQ<16>	=MEM_B_DQ<20>
CPU CHANNEL A DQS 3 -> DIMM A DQS 3		CPU CHANNEL B DQS 3 -> DIMM B DQS 3	
MEM_A_DQS_N<3>	=MEM_A_DQS_N<3>	MEM_B_DQS_N<3>	=MEM_B_DQS_N<3>
MEM_A_DQS_P<3>	=MEM_A_DQS_P<3>	MEM_B_DQS_P<3>	=MEM_B_DQS_P<3>
	GND		GND
MEM_A_DQ<31>	=MEM_A_DQ<26>	MEM_B_DQ<31>	=MEM_B_DQ<26>
MEM_A_DQ<30>	=MEM_A_DQ<24>	MEM_B_DQ<30>	=MEM_B_DQ<30>
MEM_A_DQ<29>	=MEM_A_DQ<28>	MEM_B_DQ<29>	=MEM_B_DQ<28>
MEM_A_DQ<28>	=MEM_A_DQ<25>	MEM_B_DQ<28>	=MEM_B_DQ<29>
MEM_A_DQ<27>	=MEM_A_DQ<31>	MEM_B_DQ<27>	=MEM_B_DQ<27>
MEM_A_DQ<26>	=MEM_A_DQ<27>	MEM_B_DQ<26>	=MEM_B_DQ<31>
MEM_A_DQ<25>	=MEM_A_DQ<30>	MEM_B_DQ<25>	=MEM_B_DQ<25>
MEM_A_DQ<24>	=MEM_A_DQ<29>	MEM_B_DQ<24>	=MEM_B_DQ<24>
CPU CHANNEL A DQS 4 -> DIMM A DQS 4		CPU CHANNEL B DQS 4 -> DIMM B DQS 4	
MEM_A_DQS_N<4>	=MEM_A_DQS_N<4>	MEM_B_DQS_N<4>	=MEM_B_DQS_N<4>
MEM_A_DQS_P<4>	=MEM_A_DQS_P<4>	MEM_B_DQS_P<4>	=MEM_B_DQS_P<4>
	GND		GND
MEM_A_DQ<39>	=MEM_A_DQ<38>	MEM_B_DQ<39>	=MEM_B_DQ<38>
MEM_A_DQ<38>	=MEM_A_DQ<39>	MEM_B_DQ<38>	=MEM_B_DQ<39>
MEM_A_DQ<37>	MEM_A_DQ<37>	MEM_B_DQ<37>	MEM_B_DQ<37>
MEM_A_DQ<36>	=MEM_A_DQ<33>	MEM_B_DQ<36>	=MEM_B_DQ<37>
MEM_A_DQ<35>	=MEM_A_DQ<34>	MEM_B_DQ<35>	=MEM_B_DQ<34>
MEM_A_DQ<34>	=MEM_A_DQ<35>	MEM_B_DQ<34>	=MEM_B_DQ<35>
MEM_A_DQ<33>	=MEM_A_DQ<32>	MEM_B_DQ<33>	=MEM_B_DQ<32>
MEM_A_DQ<32>	=MEM_A_DQ<36>	MEM_B_DQ<32>	=MEM_B_DQ<36>
CPU CHANNEL A DQS 5 -> DIMM A DQS 5		CPU CHANNEL B DQS 5 -> DIMM B DQS 5	
MEM_A_DQS_N<5>	=MEM_A_DQS_N<5>	MEM_B_DQS_N<5>	=MEM_B_DQS_N<5>
MEM_A_DQS_P<5>	=MEM_A_DQS_P<5>	MEM_B_DQS_P<5>	=MEM_B_DQS_P<5>
	GND		GND
MEM_A_DQ<47>	=MEM_A_DQ<46>	MEM_B_DQ<47>	=MEM_B_DQ<43>
MEM_A_DQ<46>	=MEM_A_DQ<43>	MEM_B_DQ<46>	=MEM_B_DQ<46>
MEM_A_DQ<45>	=MEM_A_DQ<45>	MEM_B_DQ<45>	=MEM_B_DQ<40>
MEM_A_DQ<44>	=MEM_A_DQ<41>	MEM_B_DQ<44>	=MEM_B_DQ<45>
MEM_A_DQ<43>	=MEM_A_DQ<47>	MEM_B_DQ<43>	=MEM_B_DQ<47>
MEM_A_DQ<42>	=MEM_A_DQ<42>	MEM_B_DQ<42>	=MEM_B_DQ<42>
MEM_A_DQ<41>	=MEM_A_DQ<40>	MEM_B_DQ<41>	=MEM_B_DQ<41>
MEM_A_DQ<40>	=MEM_A_DQ<44>	MEM_B_DQ<40>	=MEM_B_DQ<44>
CPU CHANNEL A DQS 6 -> DIMM A DQS 6		CPU CHANNEL B DQS 6 -> DIMM B DQS 6	
MEM_A_DQS_N<6>	=MEM_A_DQS_N<6>	MEM_B_DQS_N<6>	=MEM_B_DQS_N<6>
MEM_A_DQS_P<6>	=MEM_A_DQS_P<6>	MEM_B_DQS_P<6>	=MEM_B_DQS_P<6>
	GND		GND
MEM_A_DQ<55>	=MEM_A_DQ<51>	MEM_B_DQ<55>	=MEM_B_DQ<54>
MEM_A_DQ<54>	=MEM_A_DQ<54>	MEM_B_DQ<54>	=MEM_B_DQ<55>
MEM_A_DQ<53>	=MEM_A_DQ<49>	MEM_B_DQ<53>	=MEM_B_DQ<53>
MEM_A_DQ<52>	=MEM_A_DQ<53>	MEM_B_DQ<52>	=MEM_B_DQ<49>
MEM_A_DQ<51>	=MEM_A_DQ<50>	MEM_B_DQ<51>	=MEM_B_DQ<51>
MEM_A_DQ<50>	=MEM_A_DQ<55>	MEM_B_DQ<50>	=MEM_B_DQ<50>
MEM_A_DQ<49>	=MEM_A_DQ<48>	MEM_B_DQ<49>	=MEM_B_DQ<48>
MEM_A_DQ<48>	=MEM_A_DQ<52>	MEM_B_DQ<48>	=MEM_B_DQ<52>
CPU CHANNEL A DQS 7 -> DIMM A DQS 7		CPU CHANNEL B DQS 7 -> DIMM B DQS 7	
MEM_A_DQS_N<7>	=MEM_A_DQS_N<7>	MEM_B_DQS_N<7>	=MEM_B_DQS_N<7>
MEM_A_DQS_P<7>	=MEM_A_DQS_P<7>	MEM_B_DQS_P<7>	=MEM_B_DQS_P<7>
	GND		GND
MEM_A_DQ<63>	=MEM_A_DQ<58>	MEM_B_DQ<63>	=MEM_B_DQ<56>
MEM_A_DQ<62>	=MEM_A_DQ<59>	MEM_B_DQ<62>	=MEM_B_DQ<59>
MEM_A_DQ<61>	=MEM_A_DQ<60>	MEM_B_DQ<61>	=MEM_B_DQ<61>
MEM_A_DQ<60>	=MEM_A_DQ<57>	MEM_B_DQ<60>	=MEM_B_DQ<60>
MEM_A_DQ<59>	=MEM_A_DQ<63>	MEM_B_DQ<59>	=MEM_B_DQ<63>
MEM_A_DQ<58>	=MEM_A_DQ<62>	MEM_B_DQ<58>	=MEM_B_DQ<58>
MEM_A_DQ<57>	=MEM_A_DQ<61>	MEM_B_DQ<57>	=MEM_B_DQ<57>
MEM_A_DQ<56>	=MEM_A_DQ<56>	MEM_B_DQ<56>	=MEM_B_DQ<62>

NOTE: Sandybridge does not use DM signals per doc 438297 Huron River SFF DG rev1.0 Section 2.6.13

SYNC_MASTER=ANNE_K90I SYNC_DATE=06/22/2010

PAGE TITLE

DDR3 Byte/Bit Swaps

Apple Inc.

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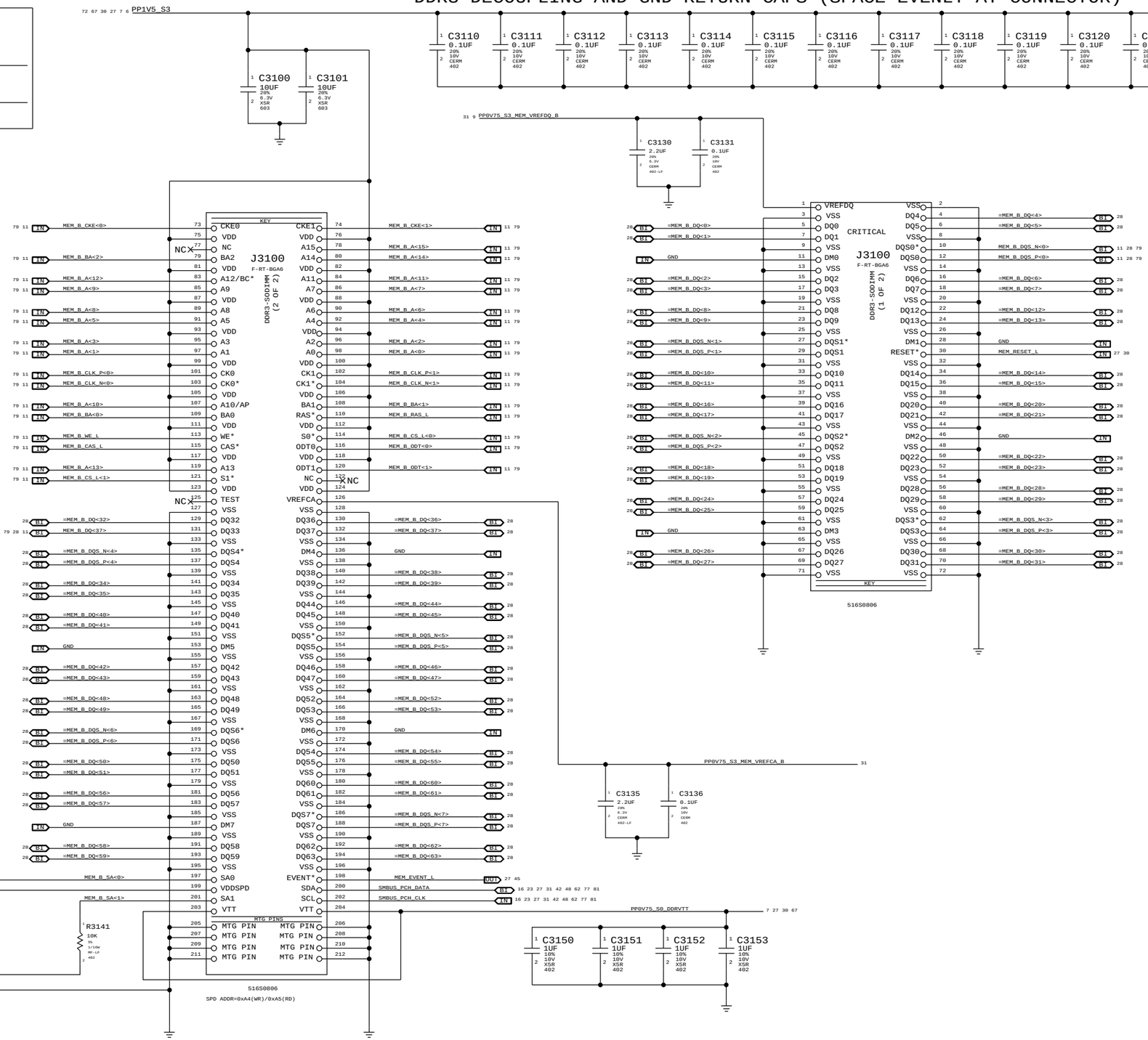
DDR3 DECOUPLING AND GND RETURN CAPS (SPACE EVENLY AT CONNECTOR)

Page Notes

Power aliases required by this page:
- =PP1V5_S0_MEM_B
- =PP1V5_S3_MEM_B
- =PP0V75_S0_MEM_VTT_B
- =PP5PO_S0_MEM_B (2.5 - 3.3V)

Signal aliases required by this page:
- =I2C_SODIMMB_SCL
- =I2C_SODIMMB_SDA

BOM options provided by this page:
(NONE)



"Expansion" (bottom) slot

SYNC_MASTER=MASTER	SYNC_DATE=MASTER
PAGE TITLE	DDR3 SO-DIMM Connector B
Apple Inc.	DRAWING NUMBER / SIZE D
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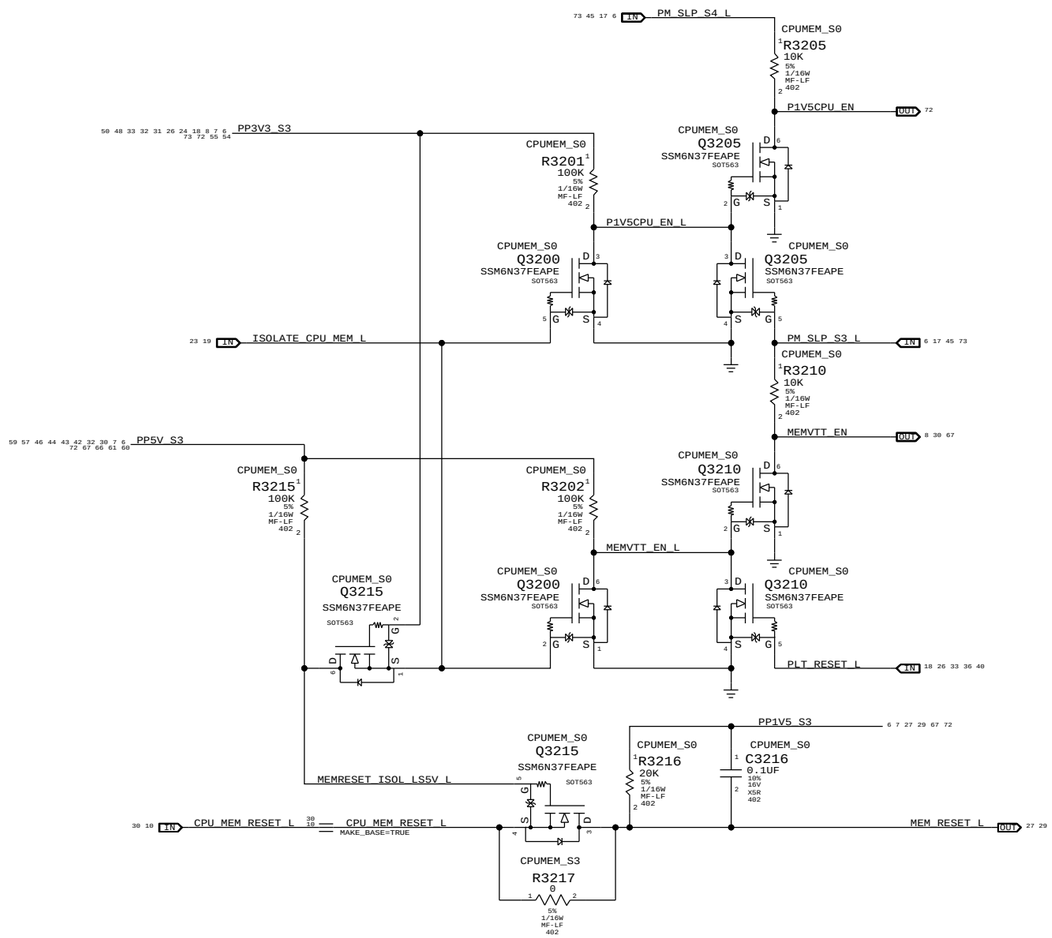
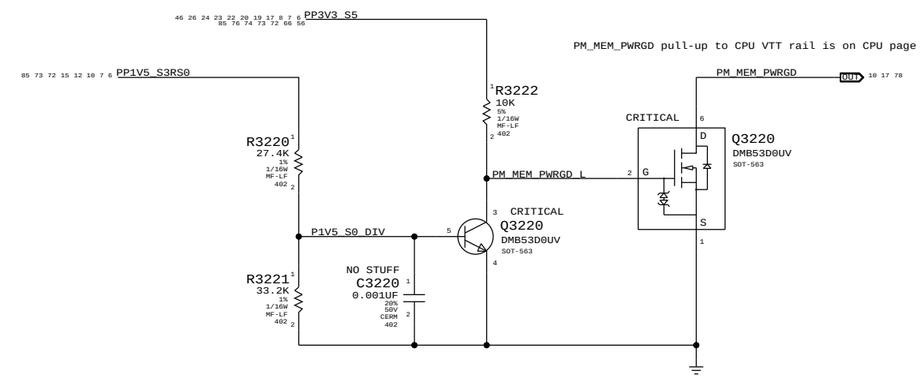
The circuit below handles CPU and VTT power during S0->S3->S0 transitions, as well as isolating the CPU's SM_DRAMRST# output from the SO-DIMMs when necessary.

ISOLATE_CPU_MEM_L GPIO state during S3<->S0 transitions determines behavior of signals.
WHEN HIGH: CPU 1.5V remains powered in S3, VTT follows S0 rails, MEM_RESET_L not isolated.
WHEN LOW: CPU 1.5V follows S0 rails, VTT ensures clean CKE transition, MEM_RESET_L isolated.

P1V5CPU_EN = (ISOLATE_CPU_MEM_L + PM_SLP_S3_L) * PM_SLP_S4_L
MEMVTT_EN = (ISOLATE_CPU_MEM_L + PLT_RST_L) * PM_SLP_S3_L
MEM_RESET_L = !ISOLATE_CPU_MEM_L + CPU_MEM_RESET_L

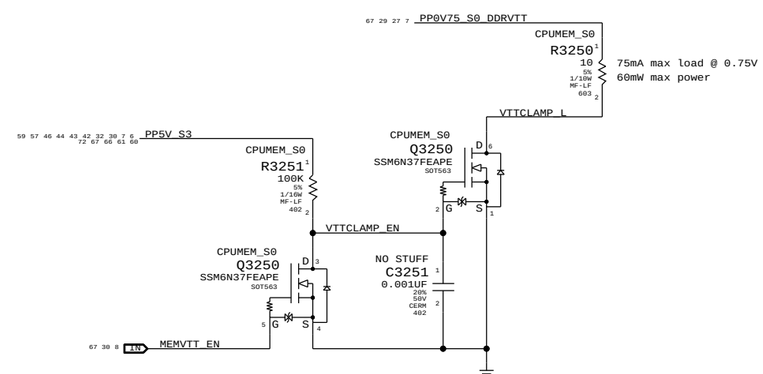


1V5 S0 "PGOOD" for CPU



MEMVTT Clamp

Ensures CKE signals are held low in S3



	Step	ISOLATE_CPU_MEM_L	PLT_RESET_L	PM_SLP_S3_L	PM_SLP_S4_L	CPU_MEM_RESET_L	MEM_RESET_L	MEMVTT_EN	P1V5CPU_EN
S0	0	1	1	1	1	1	CPU_MEM_RESET_L	1	1
	1	0	1	1	1	1	1	1	1
to	2	0	0	1	1	1	1	0	1
S3	3	0	0	0	1	X	1	0	0
	4	0	0	1	1	X	1	0	1
to	5	0	1	1	1	0 (*)	1	1	1
	6	0	1	1	1	1	1	1	1
S0	7	1	1	1	1	1	CPU_MEM_RESET_L	1	1

(*) CPU_MEM_RESET_L asserts due to loss of PM_MEM_PWRGD, must wait for software to clear before deasserting ISOLATE_CPU_MEM_L GPIO.

NOTE: In the event of a S3->S5 transition ISOLATE_CPU_MEM_L will still be asserted on next S5->S0 transition. Rails will power-up as if from S3, but MEM_RESET_L will not properly assert. Software must deassert ISOLATE_CPU_MEM_L and then generate a valid reset cycle on CPU_MEM_RESET_L.

SYNC MASTER=ANNE_K90I SYNC DATE=06/22/2010
PAGE TITLE
CPU Memory S3 Support
Apple Inc.
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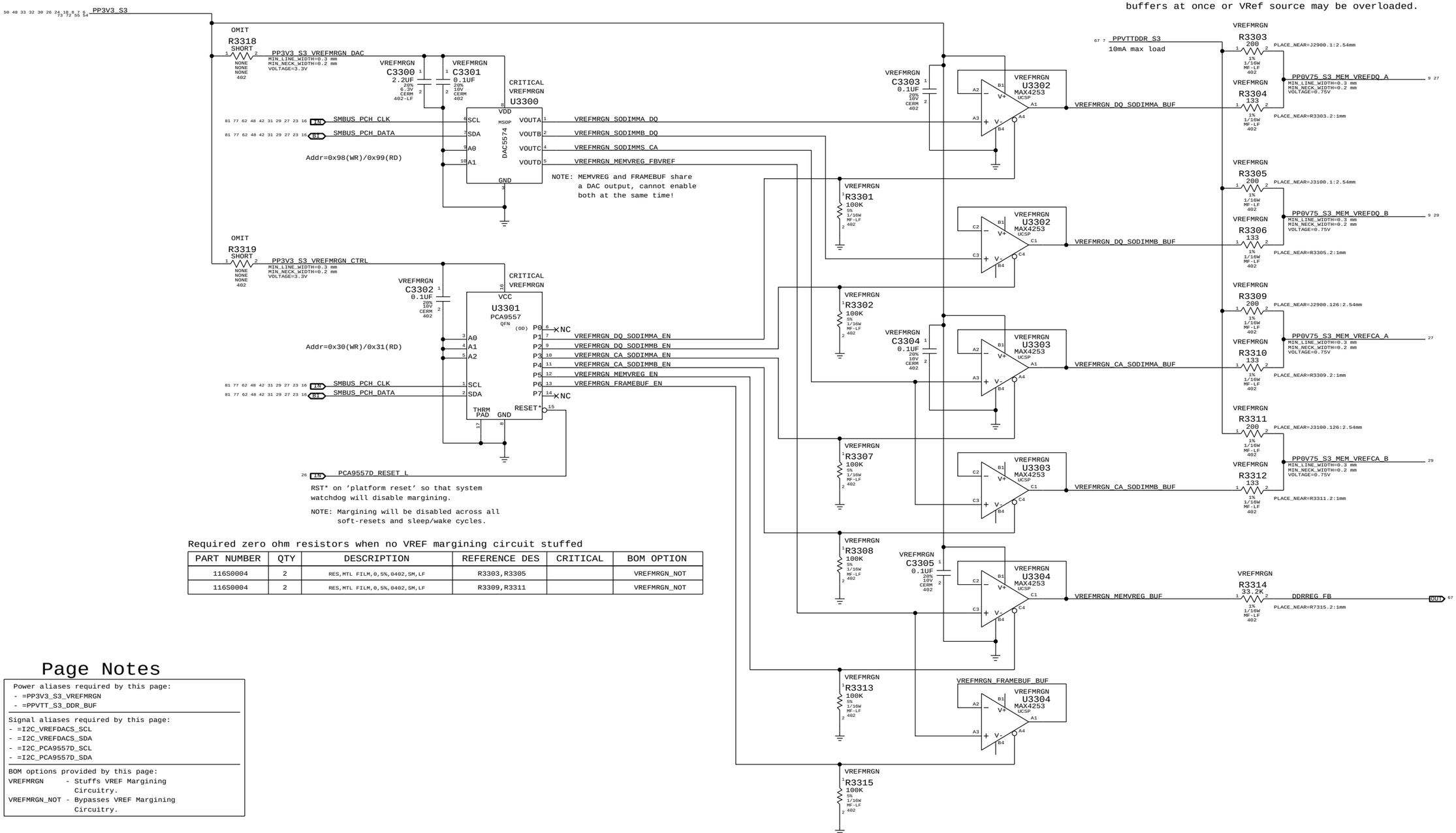
NOTE: Must not enable more than two SO-DIMM margining buffers at once or VRef source may be overloaded.



Required zero ohm resistors when no VREF margining circuit stuffed

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3303,R3305		VREFMRGN_NOT
116S0004	2	RES,MTL FILM,0,5%,0402,SM,LF	R3309,R3311		VREFMRGN_NOT

Page Notes

Power aliases required by this page:
- =PP3V3_S3_VREFMRGN
- =PPVTT_S3_DDR_BUF

Signal aliases required by this page:
- =I2C_VREFDACS_SCL
- =I2C_VREFDACS_SDA
- =I2C_PCA9557D_SCL
- =I2C_PCA9557D_SDA

BOM options provided by this page:
VREFMRGN - Stuffs VREF Margining Circuitry.
VREFMRGN_NOT - Bypasses VREF Margining Circuitry.

	MEM A VREF DQ	MEM B VREF DQ	MEM A VREF CA	MEM B VREF CA	MEM VREG	GPU Frame Buffer (1.8V, 70% VRef)
DAC Channel:	A	B	C	C	D	D
PCA9557D Pin:	1	2	3	4	5	6
Nominal value	0.75V (DAC: 0x3A)				1.5V (DAC: 0x3A)	1.267V (DAC: 0x8B)
Margined target:	0.300V - 1.200V (+/- 450mV)				1.998V - 1.002V (+/- 498mV)	1.056V - 1.442V (+/- 180mV)
DAC range:	0.000V - 1.501V (0x00 - 0x74)				0.000V - 1.501V (0x00 - 0x74)	0.000V - 3.300V (0x00 - 0xFF)
VRef current:	+3.4mA - -3.4mA (- = sourced)				+33uA - -33uA (- = sourced)	+6.0mA - -5.0mA (- = sourced)
DAC step size:	7.69mV / step @ output				8.59mV / step @ output	1.51mV / step @ output

SYNC MASTER=K91 MLB SYNC DATE=06/01/2010

PAGE TITLE
FSB/DDR3/FRAMEBUF Vref Margining

Apple Inc.

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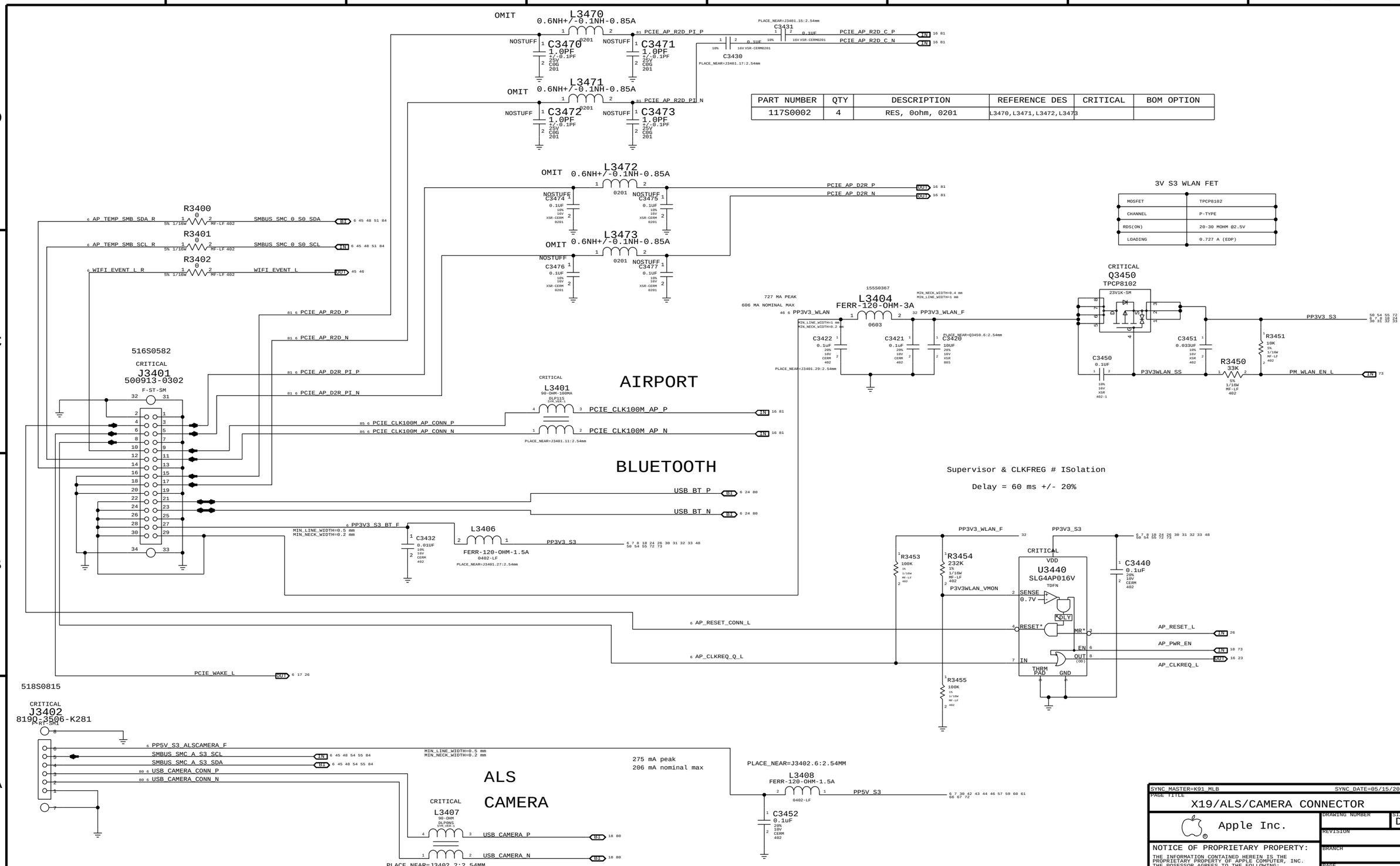

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
117S0002	4	RES, 0ohm, 0201	L3470,L3471,L3472,L3473		

SYNC MASTER=K91_MLB SYNC DATE=05/15/2016

PAGE TITLE

X19/ALS/CAMERA CONNECTOR

Apple Inc.

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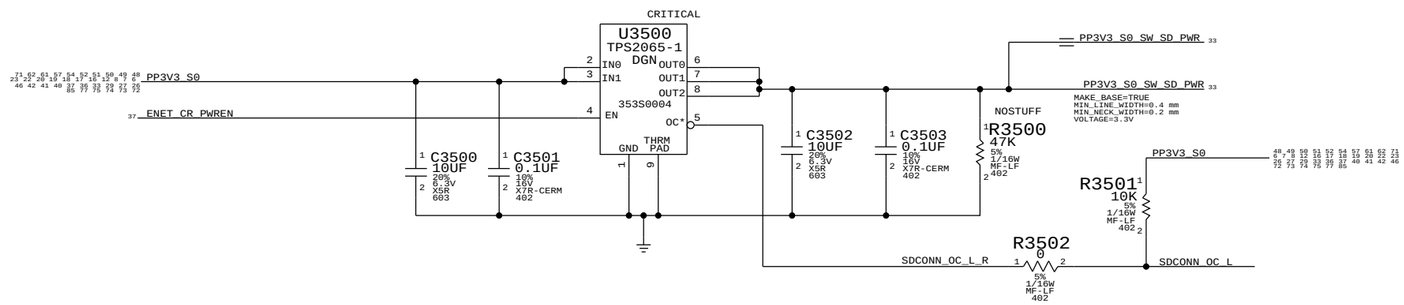
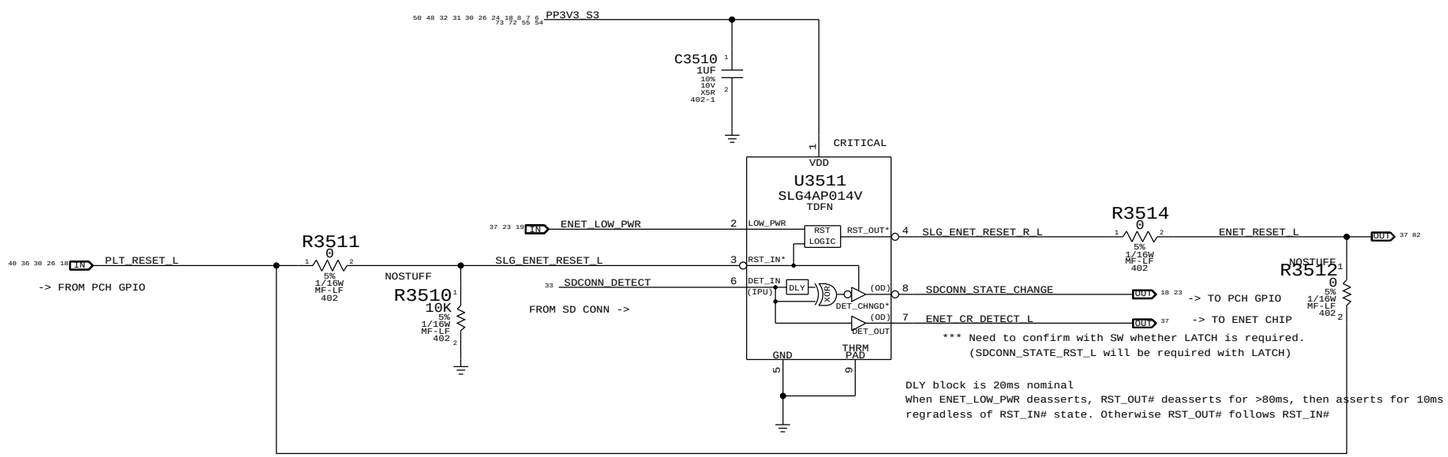
SD CARD 3.3V OVERCURRENT PROTECTION CHIP WITH ACTIVE LOAD DISCHARGE

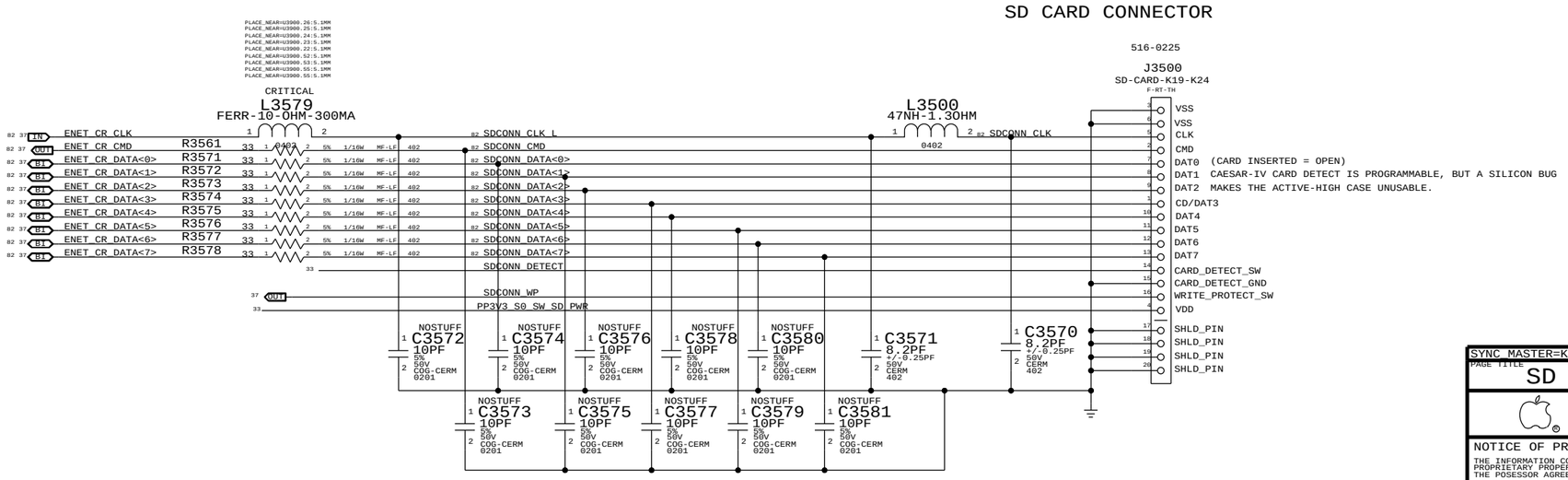
TPS2065-1 (1.0A limit) has active load discharge so R4810 is NOSTUFF.



SDCONN DETECT DEBOUNCE. ENET_RESET AND DETECT-CHANGED PCH GPIO PULSE GENERATION.



SD CARD CONNECTOR



SYNC_MASTER=K91_MLB SYNC_DATE=05/26/2010

PAGE TITLE

SD READER CONNECTOR

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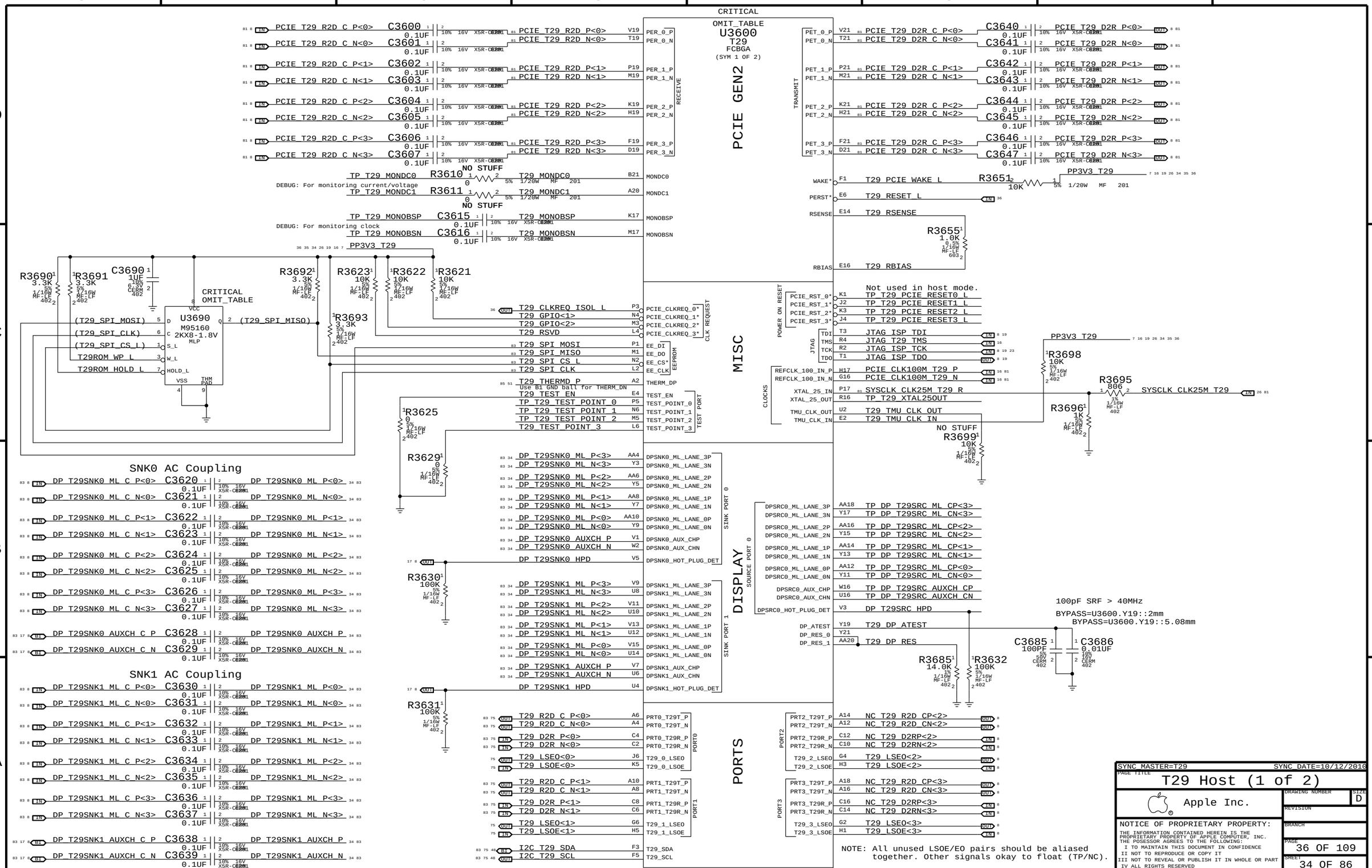

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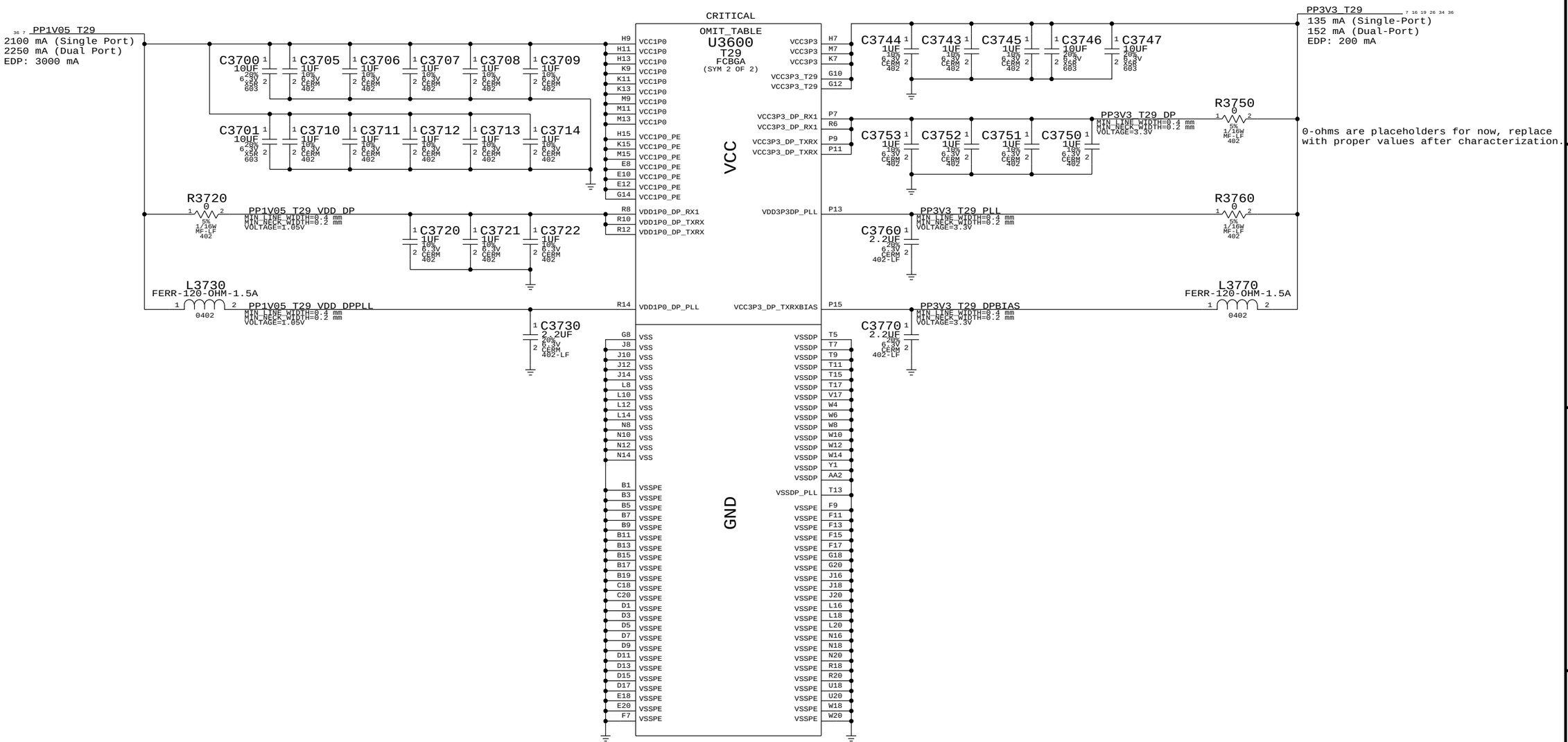

Current numbers from Vendor slide (<REDACTED> power measure 1.ppt), emailed 6/21/2010, TDP @ 90C.

SYNC_MASTER=T29 SYNC_DATE=10/12/2010

PAGE TITLE: T29 Host (2 of 2)

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DRAWING NUMBER | SIZE: D

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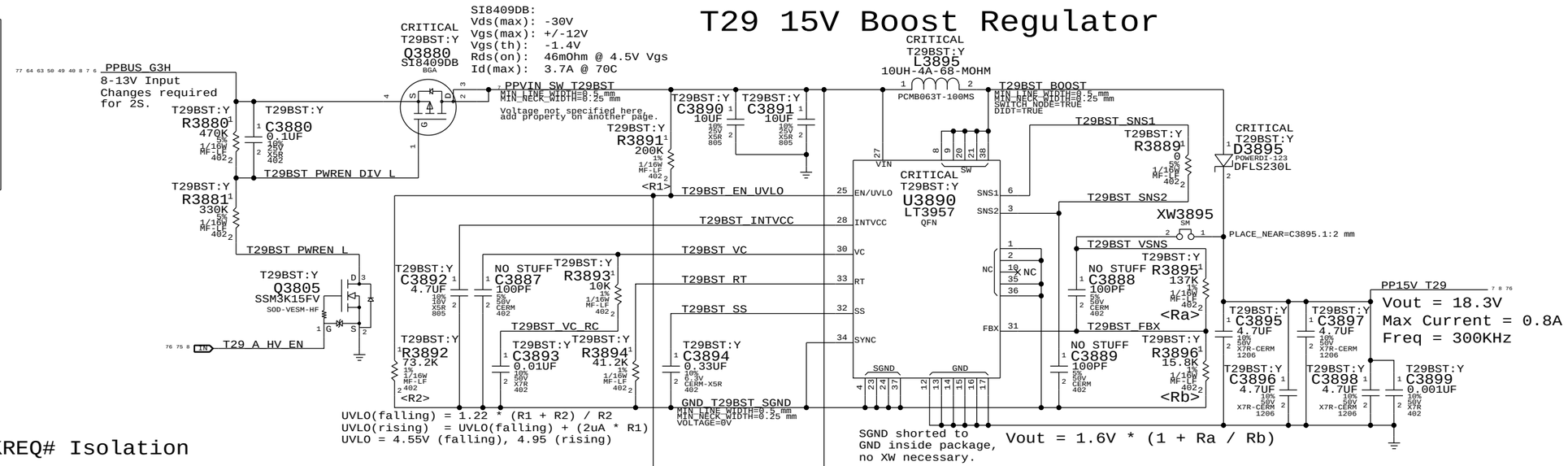
Page Notes

Power aliases required by this page:
- =PPVIN_SW_T29BST (8-13V Boost Input)
- =PP18V_T29_REG (18V Boost Output)
- =PP3V3_T29_P3V3T29FET (3.3V FET Input)
- =PP3V3_T29_FET (3.3V FET Output)
- =PP3V3_S0_T29PWRCTL
- =PP1V05_T29_P1V05T29FET (1.05V FET Input)
- =PP1V05_T29_FET (1.05V FET Output)

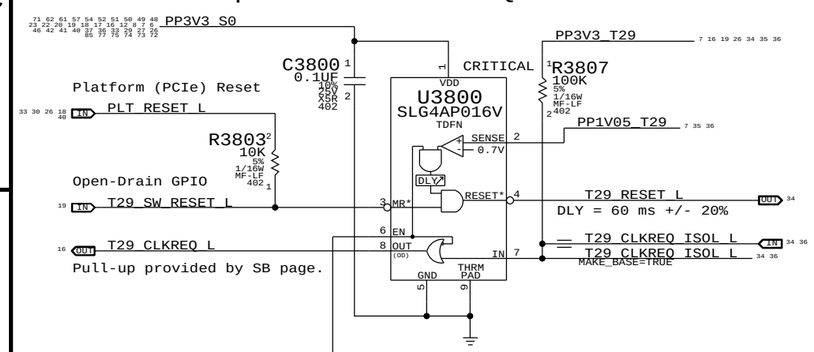
Signal aliases required by this page:
- =T29_CLKREQ_L
- =T29_RESET_L

BOM options provided by this page:
T29BST:Y - Stuffs 18V boost circuitry.

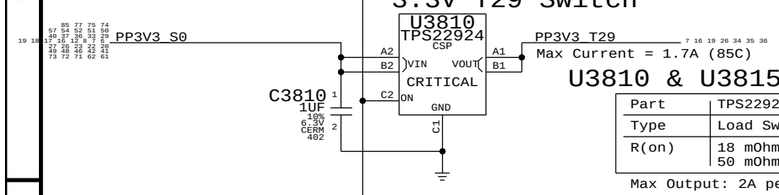
T29 15V Boost Regulator



Supervisor & CLKREQ# Isolation



3.3V T29 Switch

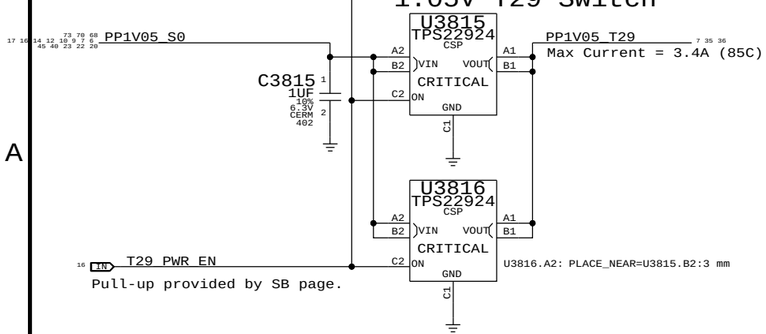


U3810 & U3815/U3816

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A per IC

1.05V T29 Switch



SYNC MASTER=T29 SYNC DATE=10/12/2010

PAGE TITLE
T29 Power Support

Apple Inc.

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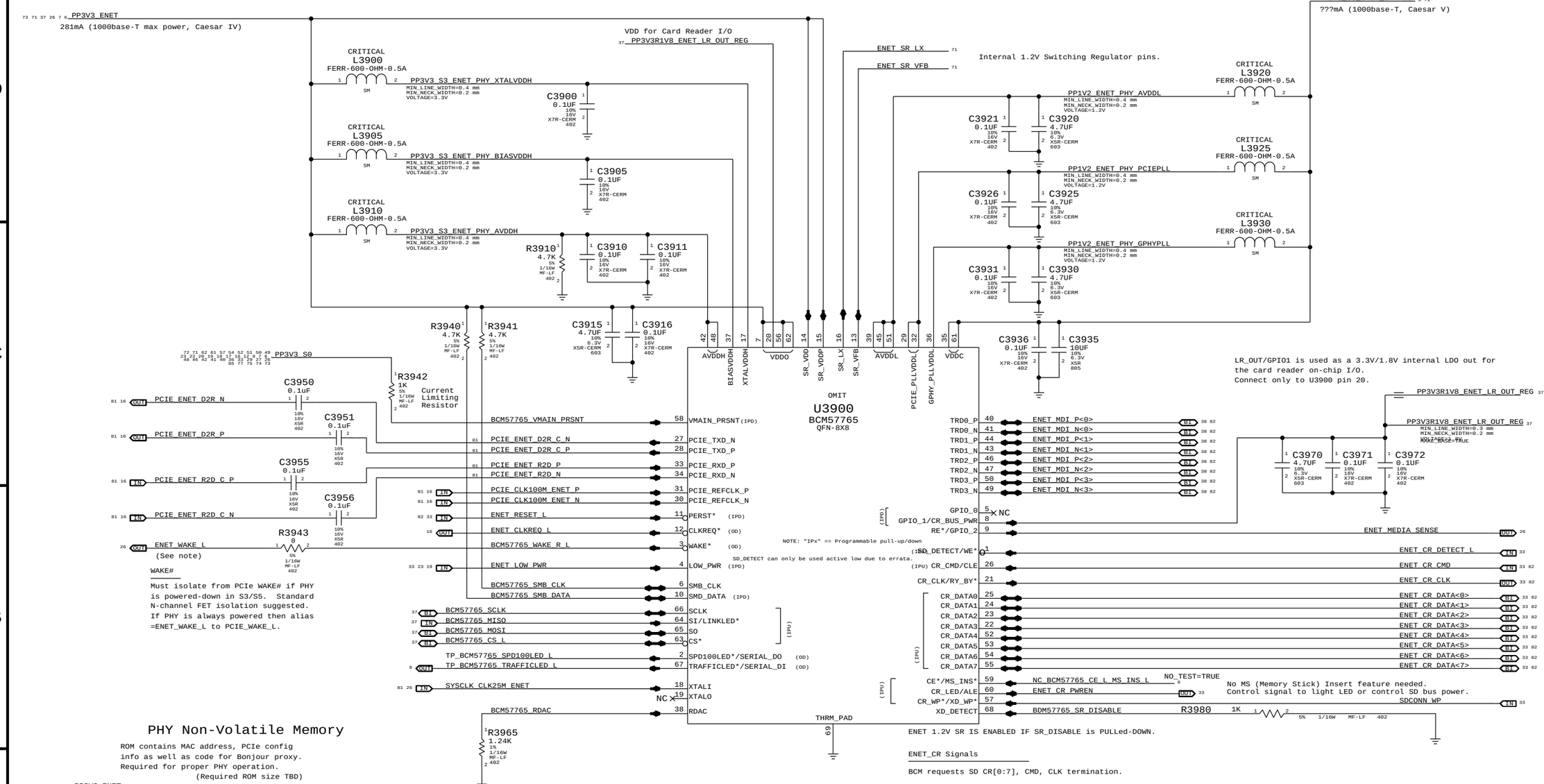
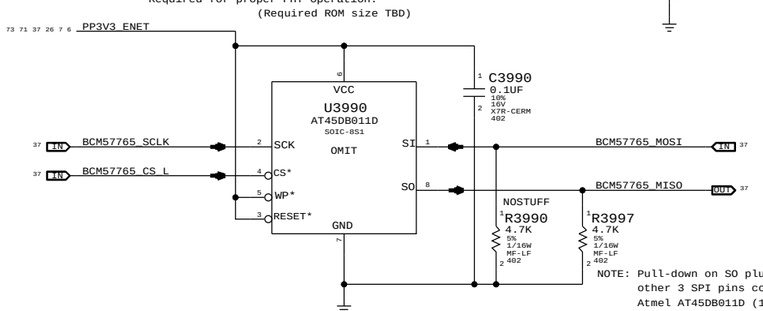
BCM57765 ENET SR pins are internal 1.2V switching regulator. See note for SR_DISABLE below.
If disabled: Okay to float VDD, VDDP & LX pin. VFB must always connect to =PP1V2_S3_ENET_PHY.
If enabled: VDD/VDDP connect to =PP3V3_S3_ENET_PHY (add bypassing), LX connects to inductor.
Special Star routing needed on these pins. Decoupling on Pg 37.



PHY Non-Volatile Memory

ROM contains MAC address, PCIe config info as well as code for Bonjour proxy. Required for proper PHY operation.
(Required ROM size TBD)



NOTE: Pull-down on SO plus internal pull-ups on other 3 SPI pins configures ENET for the Atmel AT45DB011D (1Mbit) ROM. If a different ROM is used then the straps must change.
NOTE: ENETM requires SI pull-down instead of SO.

SYNC_MASTER=K91_MLB	SYNC_DATE=05/26/2010
PAGE TITLE: ETHERNET PHY (CAESAR IV)	
Apple Inc.	DRAWING NUMBER / SIZE: D
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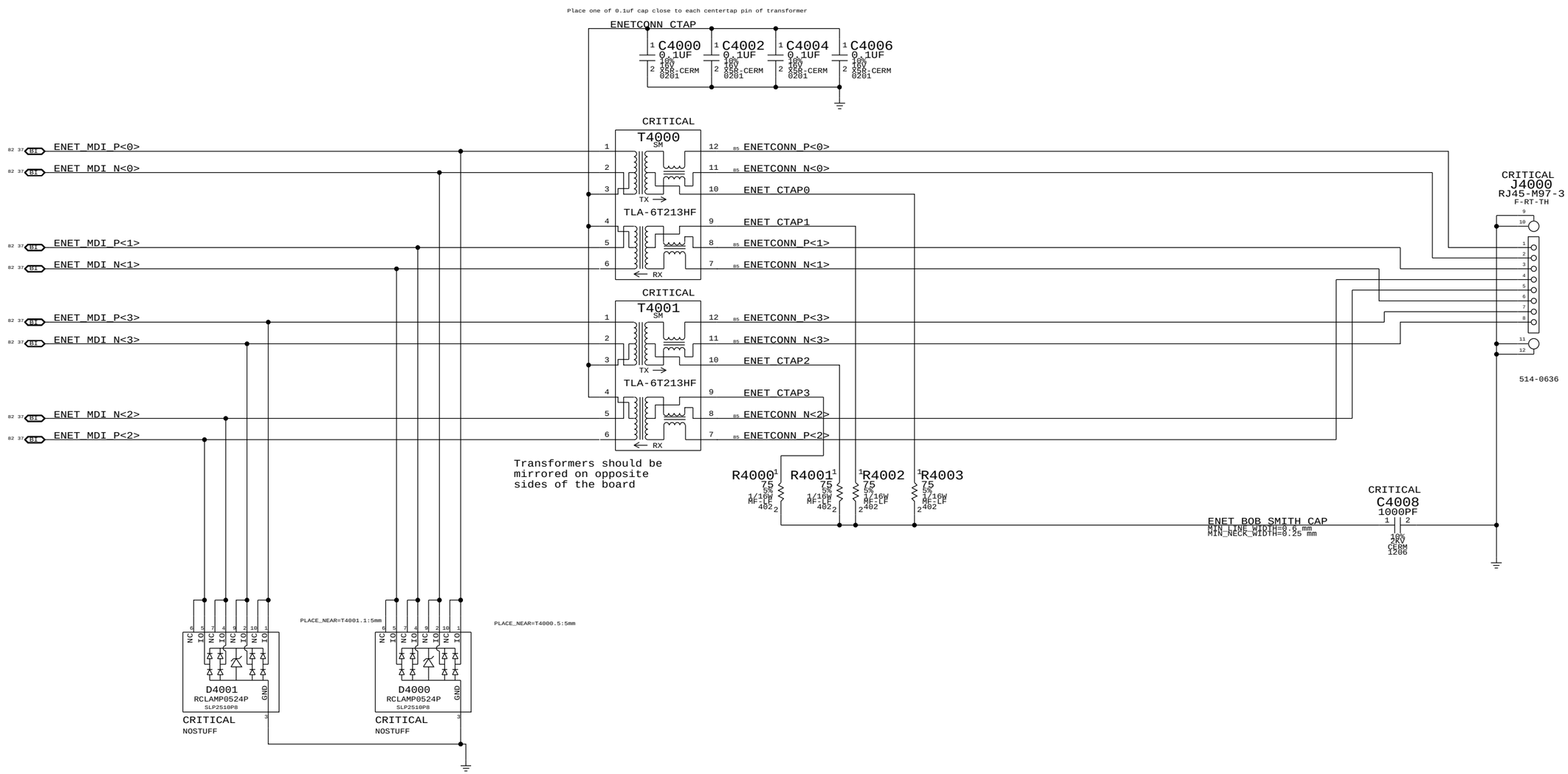
Page Notes

Power aliases required by this page:
(NONE)

Signal aliases required by this page:
(NONE)

BOM options provided by this page:
(NONE)



SYNC MASTER=K91_MLB SYNC DATE=05/26/2010

PAGE TITLE
Ethernet Connector

Apple Inc.

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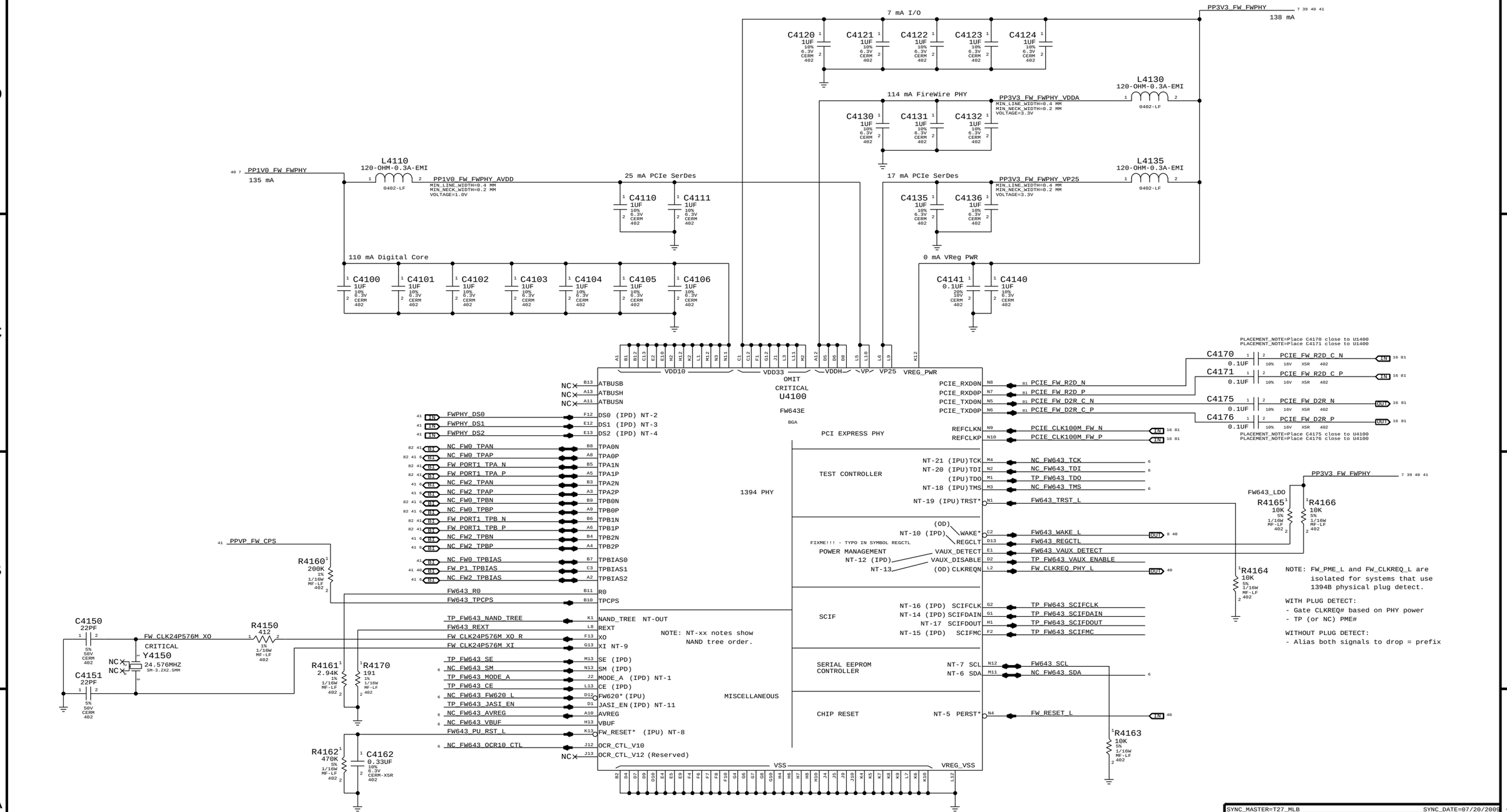

SYNC MASTER=T27_MLB SYNC DATE=07/20/2005

PAGE TITLE

FireWire LLC/PHY (FW643E)

Apple Inc.

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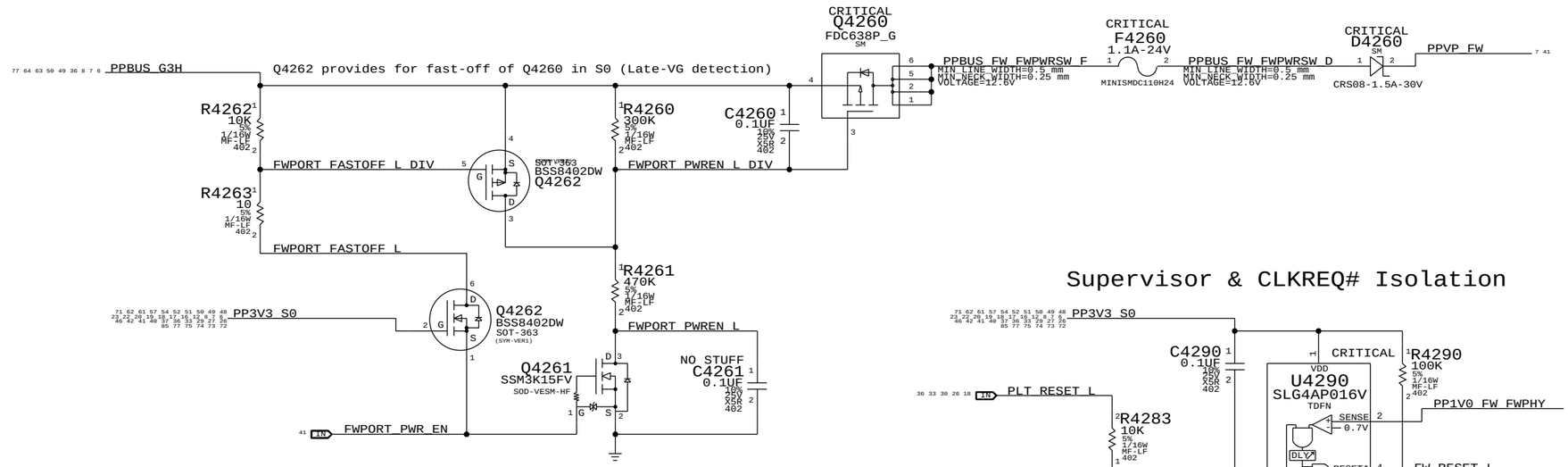
Page Notes

Power aliases required by this page:
- =PPBUS_S5_FWPWRSW (FW VP FET Input)
- =PPBUS_FW_FET (FW VP FET Output)
- =PP3V3_FW_P3V3FWFET (3.3V FET Input)
- =PP3V3_FW_FET (3.3V FET Output)
- =PP3V3_FW_FWPHY (PHY 3.3V Power)
- =PP3V3_S0_FWLATEVG
- =PP3V3_S0_FWPWRCTL
- =PP1V05_S0_FWPWRCTL (5KPD Bias Rail)
- =PP1V05_FW_P1V0FWFET (1.0V FET Input)
- =PP1V0_FW_FET_R (1.0V FET Output)
- =PP1V0_FW_FWPHY (PHY 1.0V)

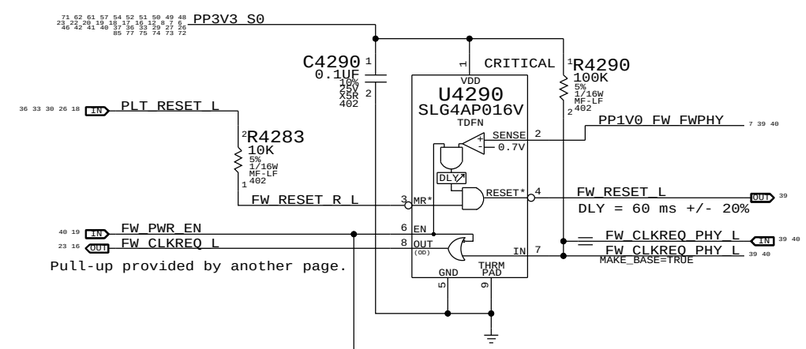
Signal aliases required by this page:
- =FW_CLKREQ_L
- =FW_PME_L

BOM options provided by this page:
(NONE)

FireWire Port Power Switch

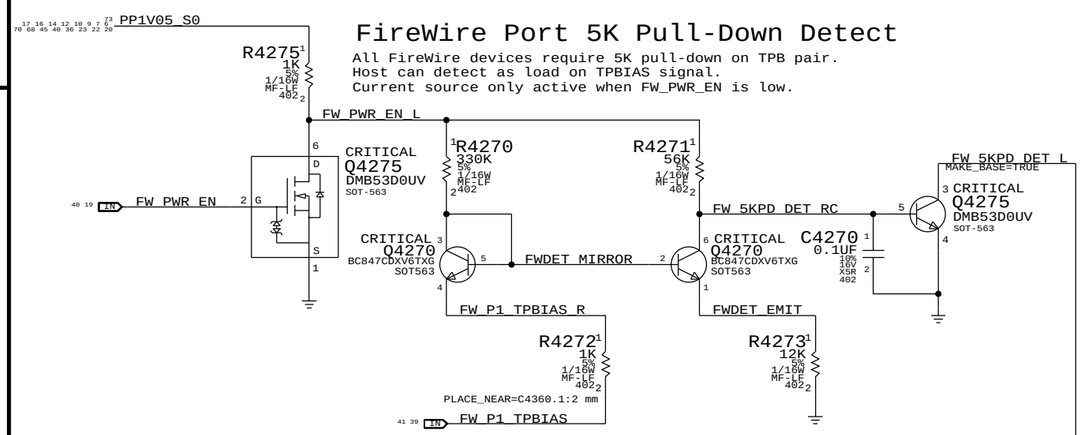


Supervisor & CLKREQ# Isolation

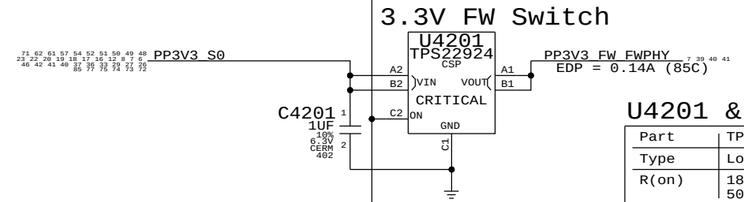


FireWire Port 5K Pull-Down Detect

All FireWire devices require 5K pull-down on TPB pair.
Host can detect as load on TPBIAS signal.
Current source only active when FW_PWR_EN is low.



3.3V FW Switch

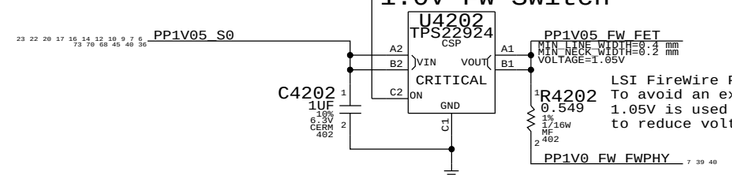


U4201 & U4202

Part	TPS22924C
Type	Load Switch
R(on)	18 mOhm Typ 50 mOhm Max

Max Output: 2A

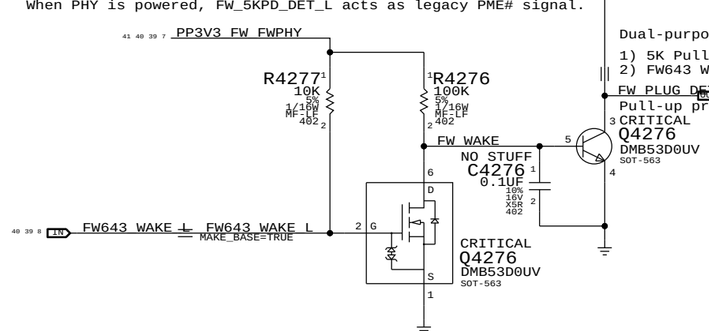
1.0V FW Switch



LSI FireWire PHY requires 1.0V.
To avoid an extra power supply,
1.05V is used with a series R
to reduce voltage.

FireWire PHY WAKE# Support

When PHY is powered, FW_5KPD_DET_L acts as legacy PME# signal.



Dual-purpose output:
1) 5K Pull-down Detect when FW_PWR_EN is low.
2) FW643 WAKE# (PME#) when PHY is powered.

Pull-up provided on another page.

TEXT NOTE FOR 3.3V RAIL CURRENT CHANGED TO EDP NUMBER.

SYNC_MASTER=T27_MLB SYNC_DATE=12/15/2009

PAGE TITLE: FireWire Port & PHY Power

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Page Notes

Power aliases required by this page:
- =PPVP_FW_PORT1
- =PPVP_FW_PHY_CPS_FET (From Port)
- =PPVP_FW_PHY_CPS (To PHY)
- =PP3V3_FW_FWPHY
- =PP3V3_S0_FWLATEVG

Signal aliases required by this page:
- =FW_PHY_DS0
- =FW_PHY_DS1
- =FW_PHY_DS2

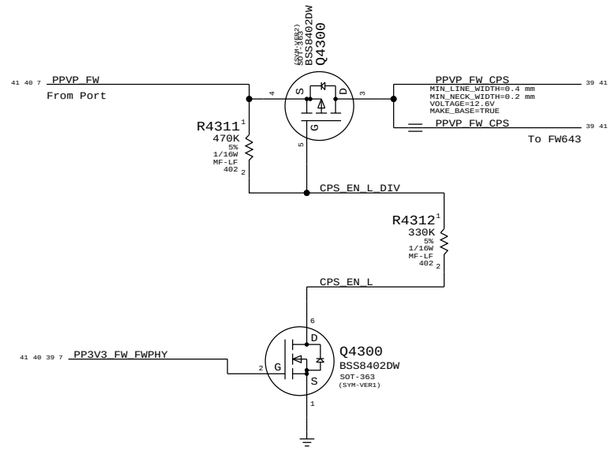
NOTE: This page is expected to contain the necessary aliases to map the FireWire TPA/TPB pairs to their appropriate connectors and/or to properly terminate unused signals.

BOM options provided by this page:
(NONE)

1394b implementation based on Apple FireWire Design Guide (FWDG 0.6, 5/14/03)

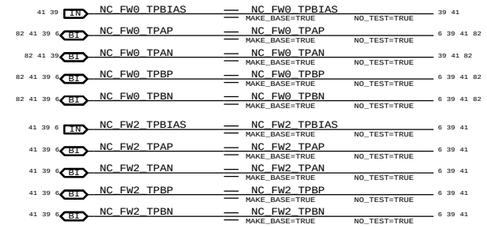
FW643 TPCPS Leakage Protection

FW643 has internal leakage path from TPCPS pin to VDD33.
FET blocks current to TPCPS until VDD33 is powered.



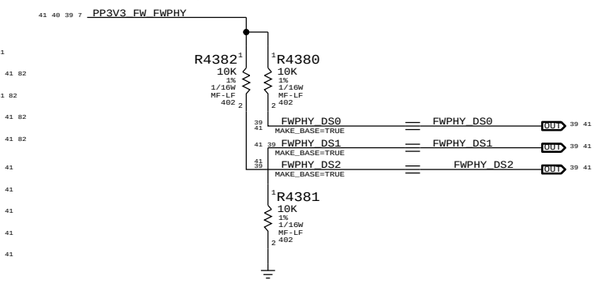
Unused FireWire Ports

Disabled per LSI instructions
(All unused port signals TP/NC)



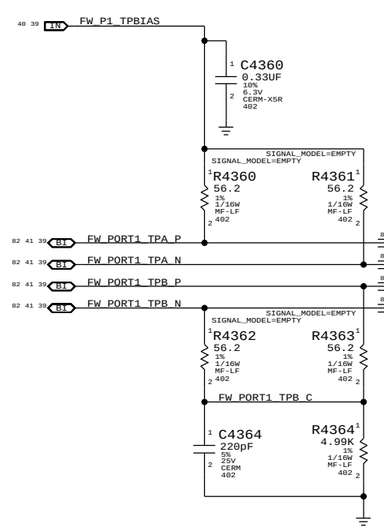
FireWire PHY Config Straps

Configures PHY for:
- Port "1" Bilingual (1394B)

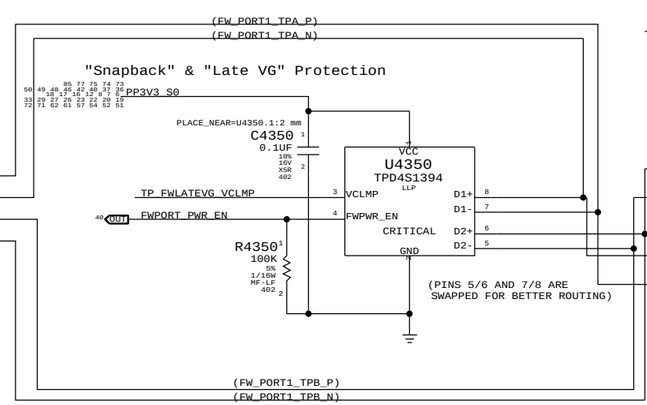


Termination

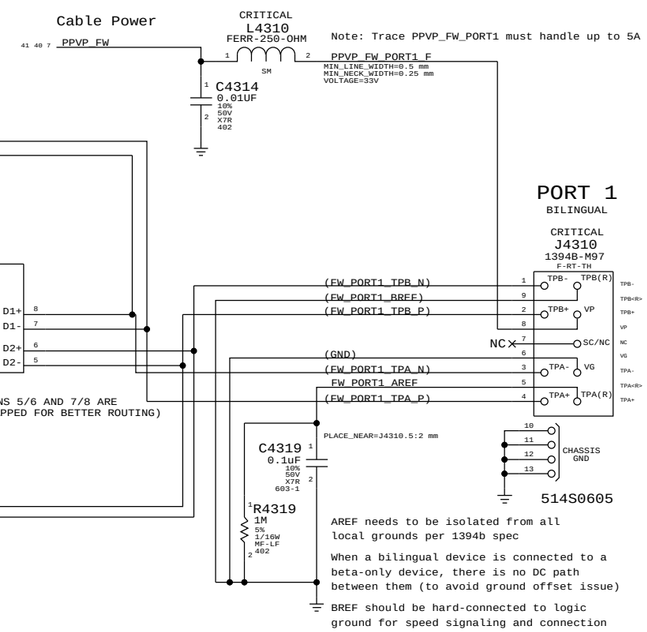
Place close to FireWire PHY



"Snapback" & "Late VG" Protection



Cable Power



Note: Trace PPVP_FW_PORT1 must handle up to 5A

AREF needs to be isolated from all local grounds per 1394b spec

When a bilingual device is connected to a beta-only device, there is no DC path between them (to avoid ground offset issue)

BREF should be hard-connected to logic ground for speed signaling and connection

CANNOT SYNC THIS PAGE FROM T27, TPA AND TPB FOR U4350 IS SWAPPED

SYNC_MASTER=T27_MLB SYNC_DATE=07/28/2009

PAGE TITLE: FireWire Connector

Apple Inc.

DRAWING NUMBER | SIZE: D

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PAGE: 43 OF 109

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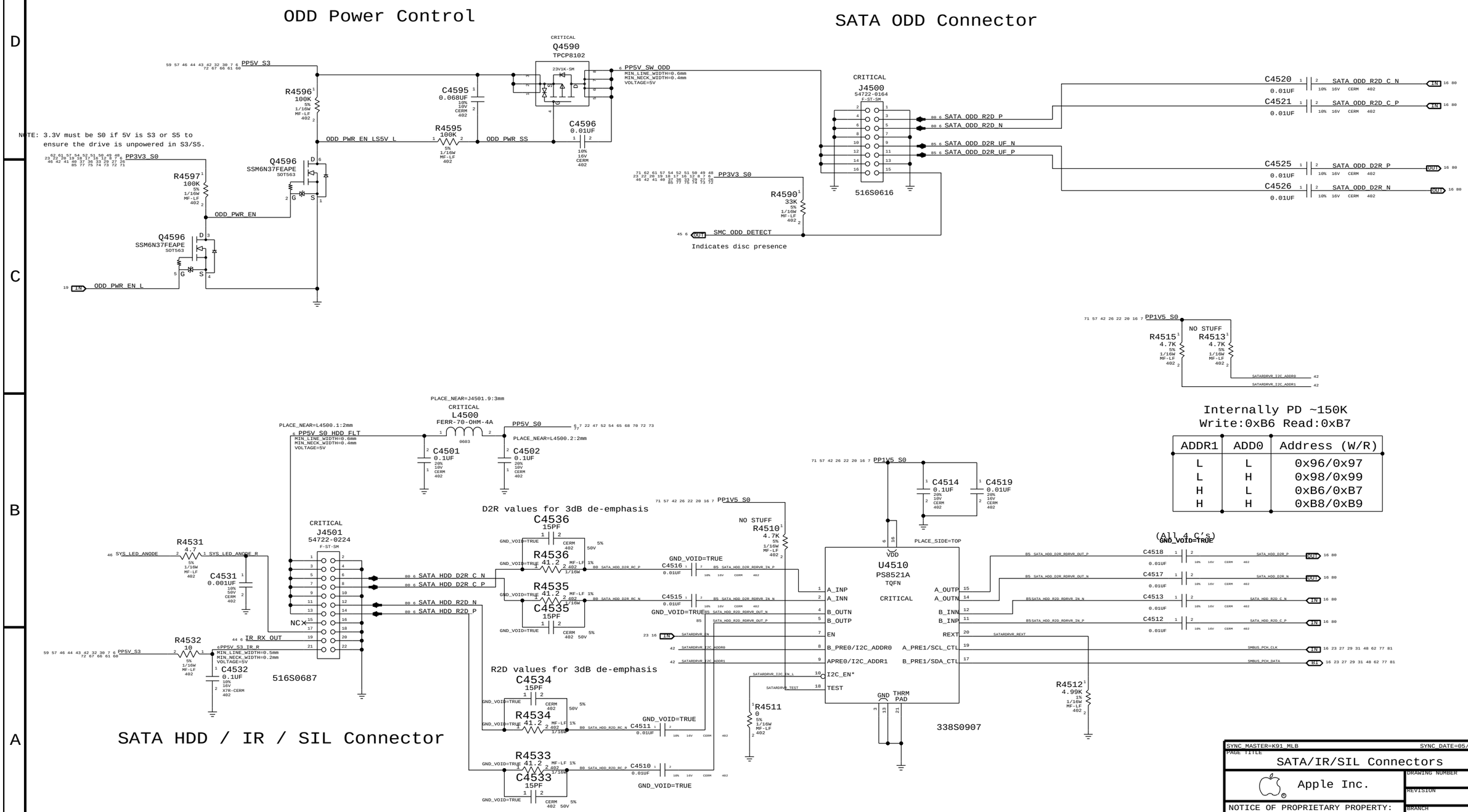

SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

PAGE TITLE: SATA/IR/SIL Connectors

Apple Inc.

DRAWING NUMBER: SIZE D

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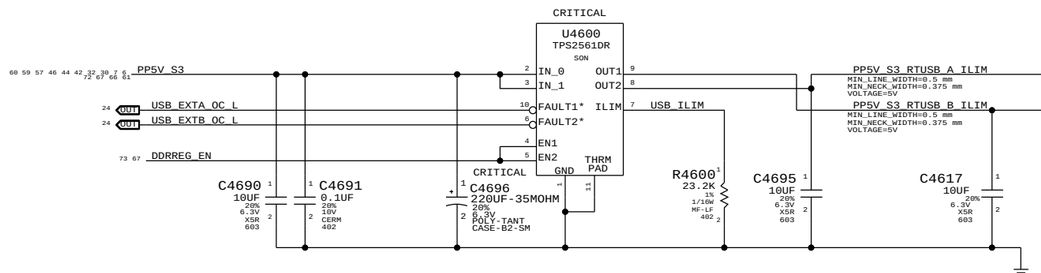
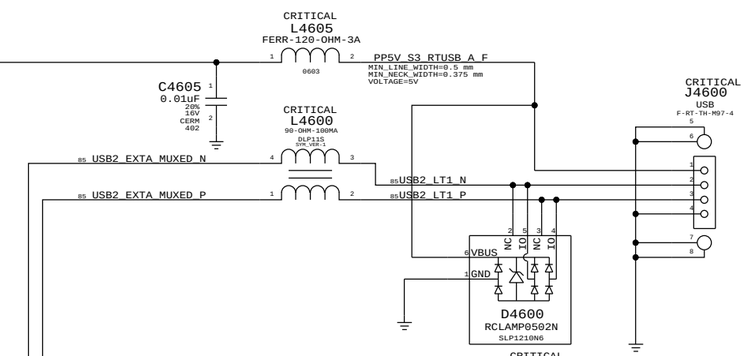
USB Port Power Switch



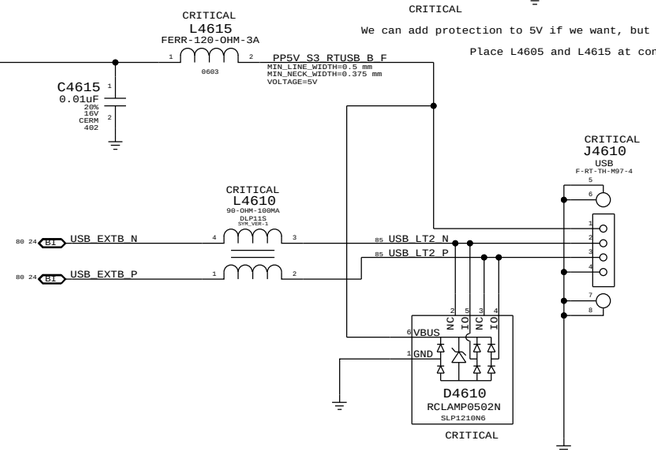
Current limit per port (R4600): 2.18A min / 2.63A max

Left USB Port A

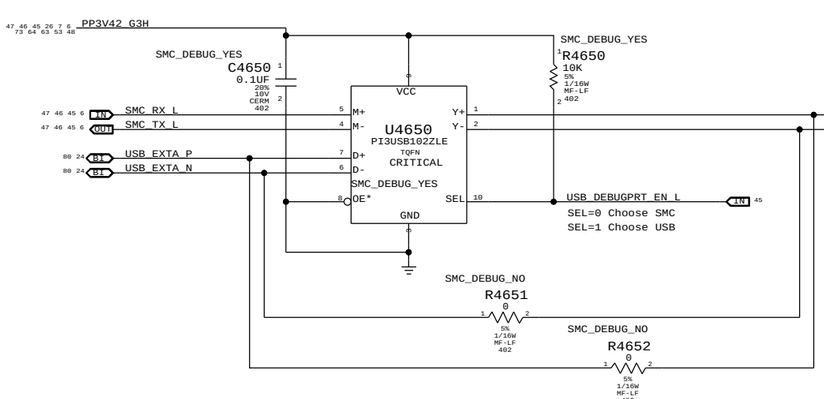


We can add protection to 5V if we want, but leaving NC for now

Place L4605 and L4615 at connector pin



USB/SMC Debug Mux



Left USB Port B

SYNC_MASTER=K91_MLB SYNC_DATE=06/01/2010

PAGE TITLE

External USB Connectors

Apple Inc.

DRAWING NUMBER

SIZE D

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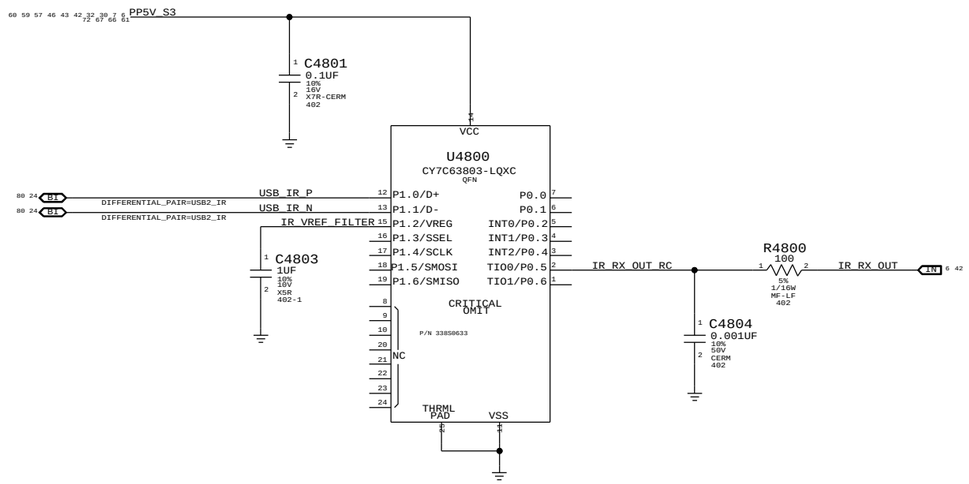
IR SUPPORT



SYNC_MASTER=K91_MLB SYNC_DATE=05/15/2010

PAGE TITLE

Front Flex Support

Apple Inc.

DRAWING NUMBER

SIZE D

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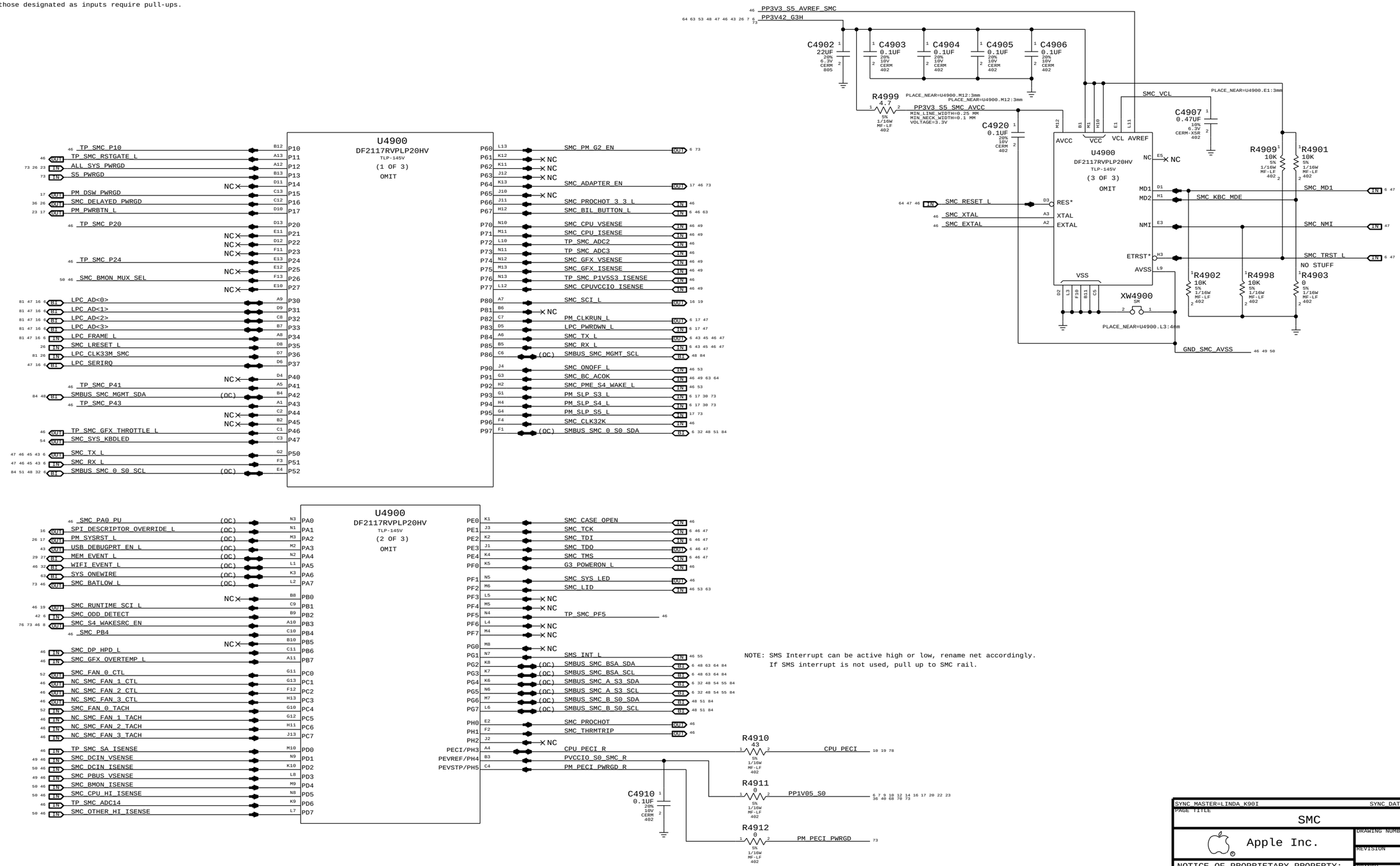
NOTE: Unused pins have "SMC_Pxx" names. Unused pins designed as outputs can be left floating, those designated as inputs require pull-ups.



NOTE: SMS Interrupt can be active high or low, rename net accordingly.
If SMS interrupt is not used, pull up to SMC rail.

SYNC_MASTER=LINDA_K90I SYNC_DATE=07/07/2010

PAGE TITLE

SMC

Apple Inc.

DRAWING NUMBER

SIZE D

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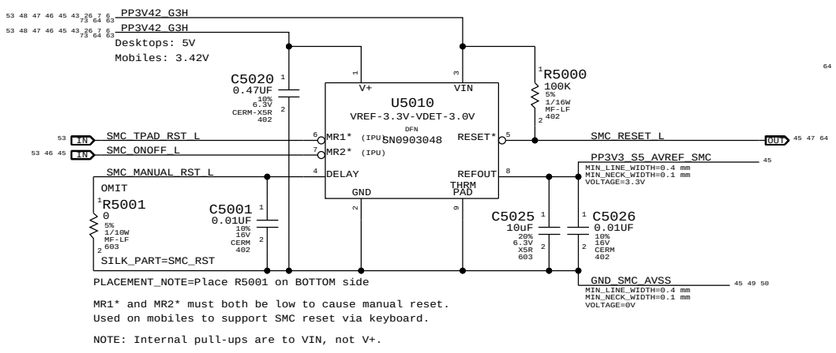
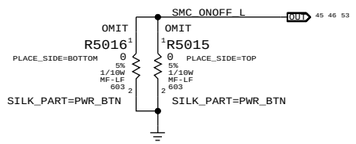
SMC Reset "Button", Supervisor & AVREF Supply



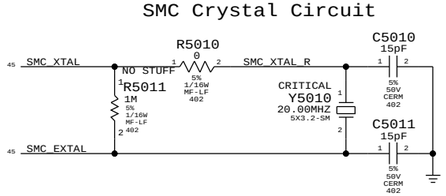
MR1* and MR2* must both be low to cause manual reset.
Used on mobiles to support SMC reset via keyboard.

NOTE: Internal pull-ups are to VIN, not V+.

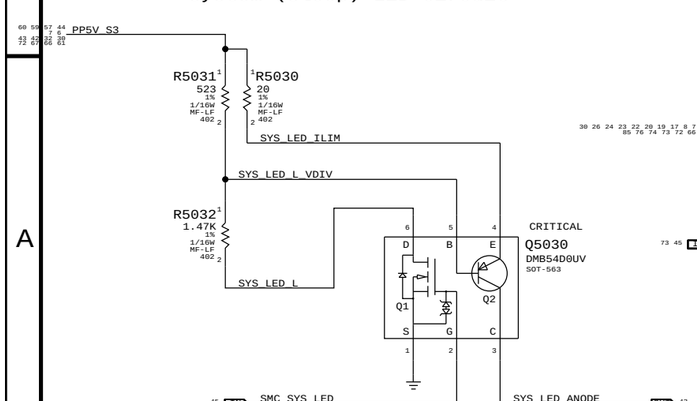
Debug Power "Buttons"



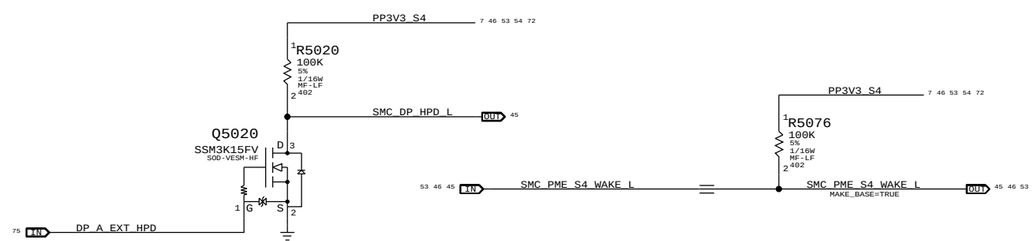
SMC Crystal Circuit



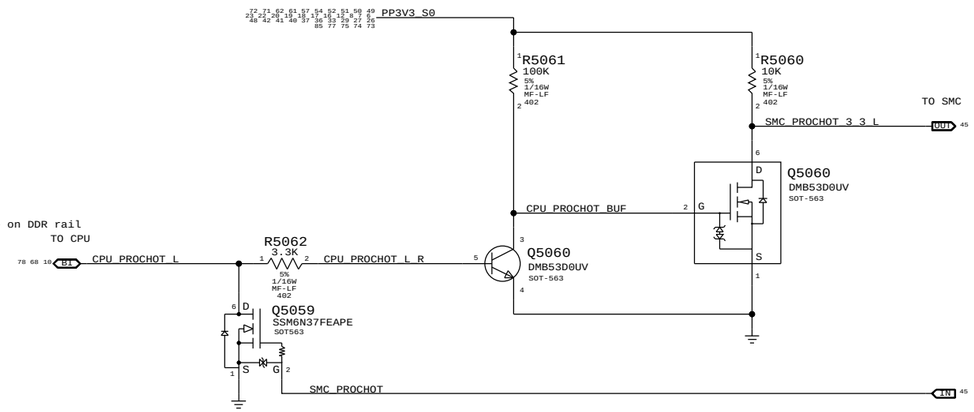
System (Sleep) LED Circuit

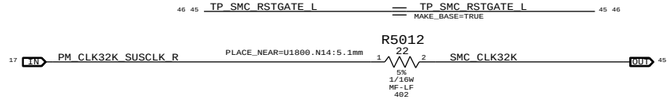


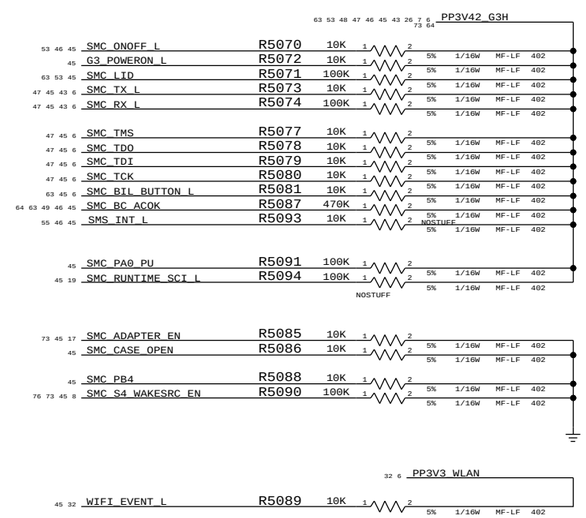
NC_SMC_FAN_2_CTL	NC_SMC_FAN_2_CTL	MAKE_BASE=TRUE	
NC_SMC_FAN_2_TACH	NC_SMC_FAN_2_TACH	MAKE_BASE=TRUE	
NC_SMC_FAN_3_CTL	NC_SMC_FAN_3_CTL	MAKE_BASE=TRUE	
NC_SMC_FAN_3_TACH	NC_SMC_FAN_3_TACH	MAKE_BASE=TRUE	
SMC_BC_ACOK	SMC_BC_ACOK	MAKE_BASE=TRUE	
SMS_INT_L	SMS_INT_L	MAKE_BASE=TRUE	
SMC_CPU_VSENSE	SMC_CPU_VSENSE	MAKE_BASE=TRUE	
SMC_CPU_ISENSE	SMC_CPU_ISENSE	MAKE_BASE=TRUE	
SMC_GFX_VSENSE	SMC_GFX_VSENSE	MAKE_BASE=TRUE	
SMC_GFX_ISENSE	SMC_GFX_ISENSE	MAKE_BASE=TRUE	confirm if K90 needs Isense on DDR rail
TP_SMC_P1V5S3_ISENSE	TP_SMC_P1V5S3_ISENSE	MAKE_BASE=TRUE	
SMC_CPUVCCIO_ISENSE	SMC_CPUVCCIO_ISENSE	MAKE_BASE=TRUE	
TP_SMC_SA_ISENSE	TP_SMC_SA_ISENSE	MAKE_BASE=TRUE	
SMC_DCIN_VSENSE	SMC_DCIN_VSENSE	MAKE_BASE=TRUE	
SMC_DCIN_ISENSE	SMC_DCIN_ISENSE	MAKE_BASE=TRUE	
SMC_PBUS_VSENSE	SMC_PBUS_VSENSE	MAKE_BASE=TRUE	
SMC_BMON_ISENSE	SMC_BMON_ISENSE	MAKE_BASE=TRUE	
SMC_CPU_HI_ISENSE	SMC_CPU_HI_ISENSE	MAKE_BASE=TRUE	
SMC_OTHER_HI_ISENSE	SMC_OTHER_HI_ISENSE	MAKE_BASE=TRUE	
TP_SMC_P10	TP_SMC_P10	MAKE_BASE=TRUE	
TP_SMC_P20	TP_SMC_P20	MAKE_BASE=TRUE	
TP_SMC_P24	TP_SMC_P24	MAKE_BASE=TRUE	
SMC_BMON_MUX_SEL	SMC_BMON_MUX_SEL	MAKE_BASE=TRUE	
TP_SMC_P41	TP_SMC_P41	MAKE_BASE=TRUE	
TP_SMC_P43	TP_SMC_P43	MAKE_BASE=TRUE	
TP_SMC_PF5	TP_SMC_PF5	MAKE_BASE=TRUE	
TP_SMC_RSTGATE_L	TP_SMC_RSTGATE_L	MAKE_BASE=TRUE	



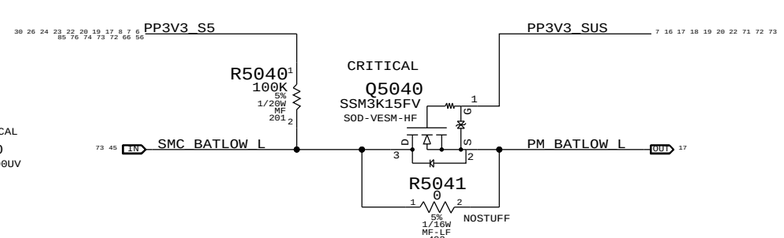
SMC FSB to 3.3V Level Shifting







BATLOW# Isolation



Internal 20K pull-up on PM_BATLOW_L in PCH.

Below connections are different from K91

NC_SMC_FAN_1_CTL	NC_SMC_FAN_1_CTL	MAKE_BASE=TRUE	
NC_SMC_FAN_1_TACH	NC_SMC_FAN_1_TACH	MAKE_BASE=TRUE	
TP_SMC_ADC2	TP_SMC_ADC2	MAKE_BASE=TRUE	
TP_SMC_ADC3	TP_SMC_ADC3	MAKE_BASE=TRUE	
TP_SMC_ADC14	TP_SMC_ADC14	MAKE_BASE=TRUE	
TP_SMC_GFX_THROTTLE_L	TP_SMC_GFX_THROTTLE_L	MAKE_BASE=TRUE	

SMC_GFX_OVERTEMP_L R5095 10K PP3V42_G3H 5% 1/16W MF-LF 402

SYNC_MASTER=LINDA_K90I SYNC_DATE=07/08/2016

PAGE TITLE: SMC Support

Apple Inc.

DRAWING NUMBER | SIZE D

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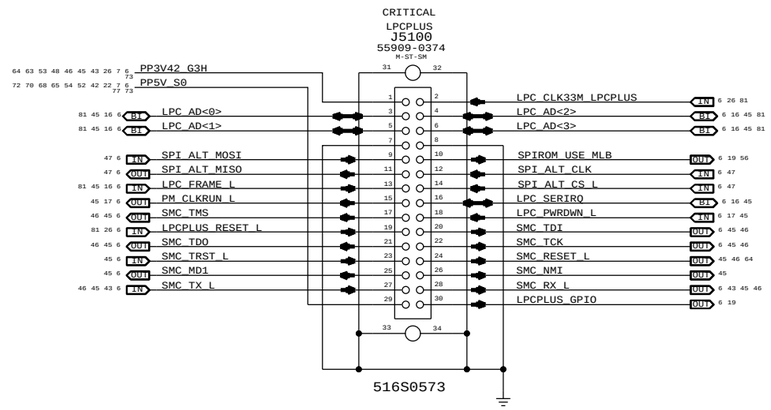
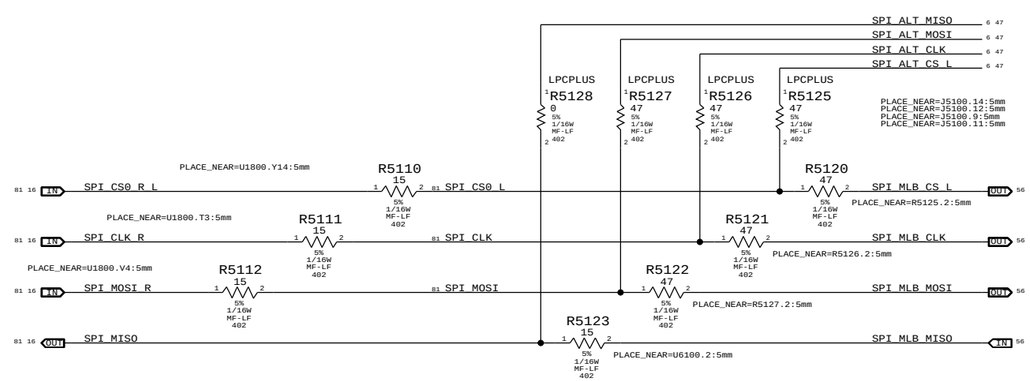
LPC+SPI Connector



SPI Bus Series Termination



SYNC MASTER=K91_MLB SYNC DATE=05/15/2010

PAGE TITLE

LPC+SPI Debug Connector

Apple Inc.

DRAWING NUMBER

SIZE D

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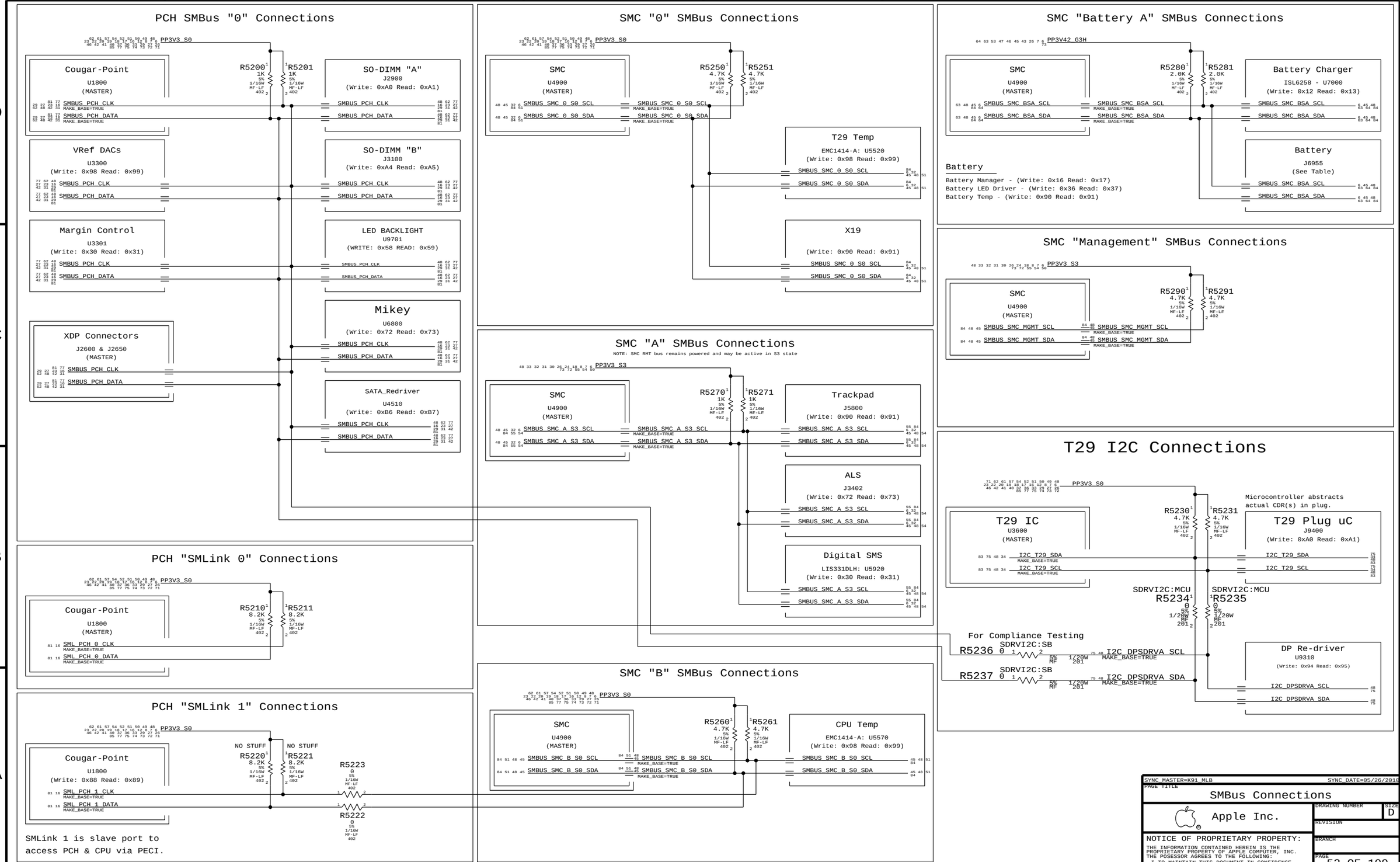

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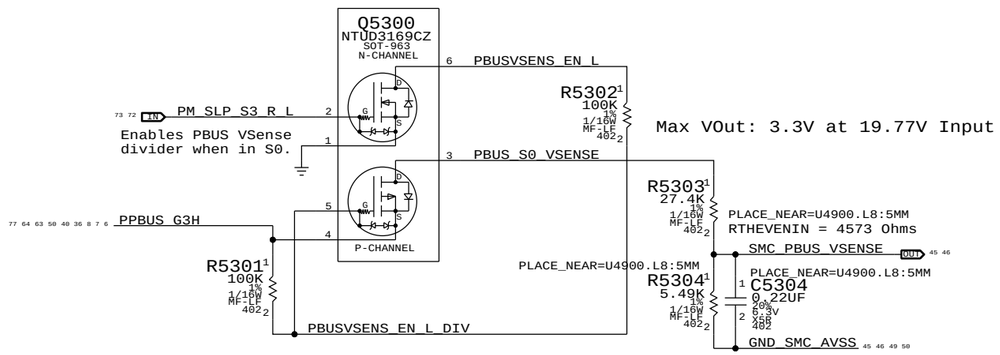
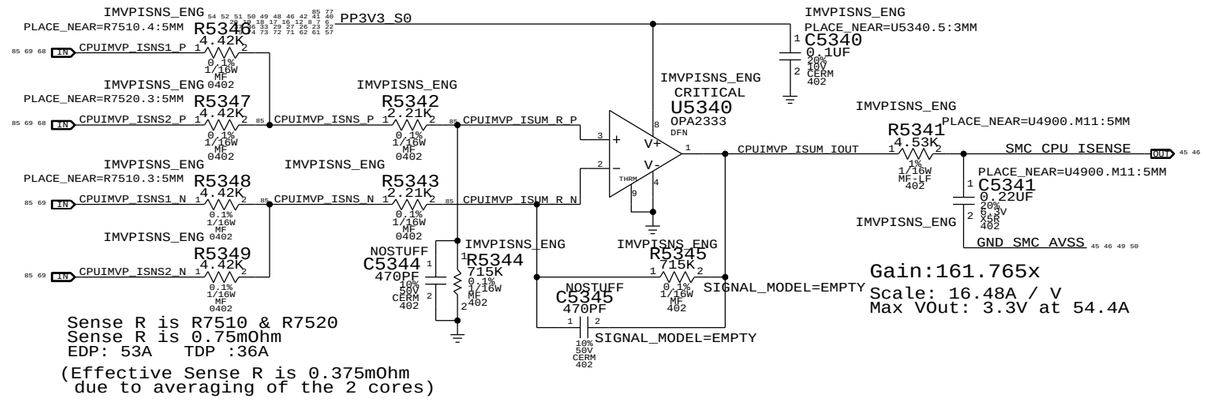
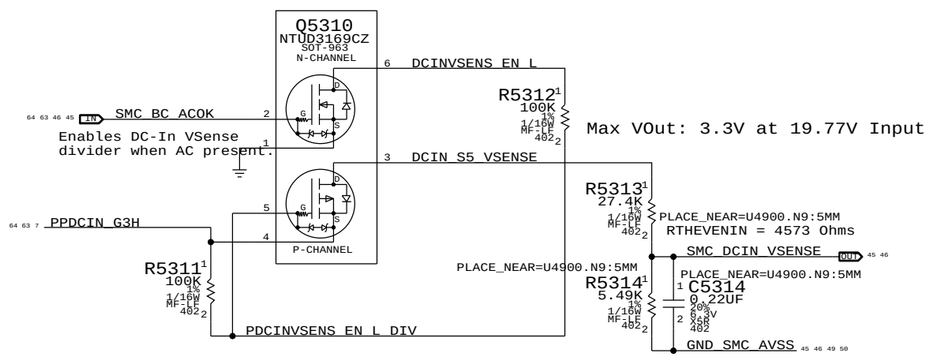
PBUS Voltage Sense Enable & Filter



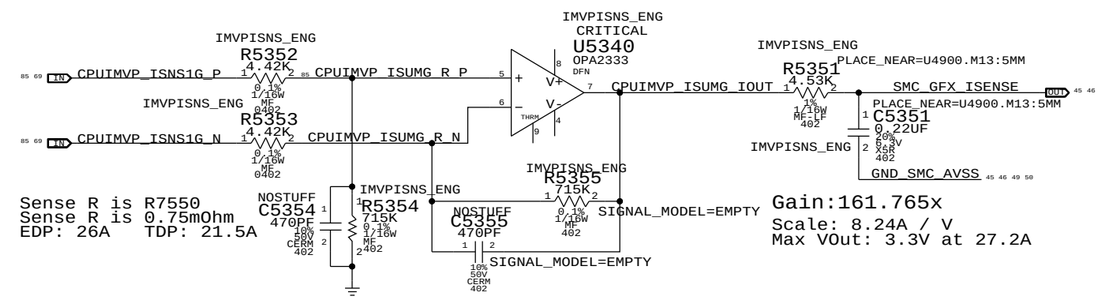
CPU VCore Load Side Current Sense / Filter



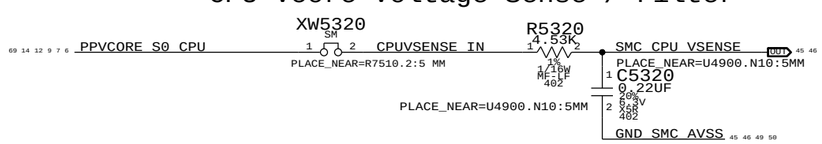
DC-In Voltage Sense Enable & Filter



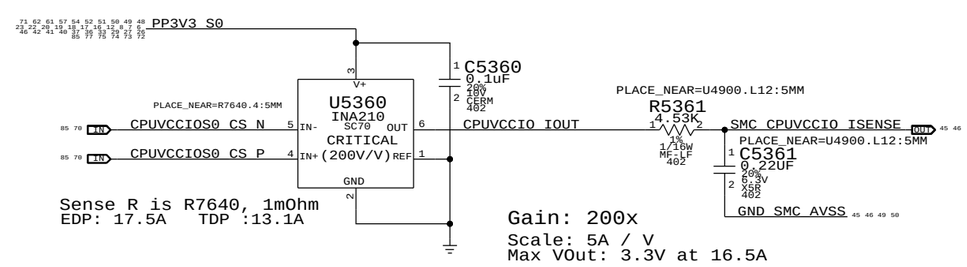
GFX/IG VCore Load Side Current Sense / Filter



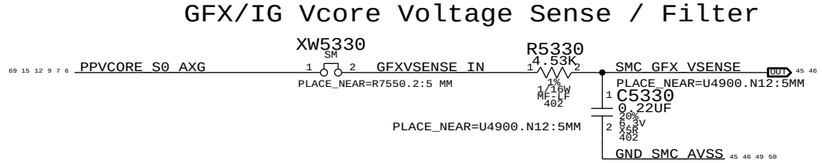
CPU Vcore Voltage Sense / Filter



CPU 1.05V VCCIO Current Sense / Filter



GFX/IG Vcore Voltage Sense / Filter



SYNC MASTER=LINDA K90I SYNC DATE=10/22/2010

PAGE TITLE: Voltage & Load Side Current Sensing

Apple Inc.

DRAWING NUMBER | SIZE: D

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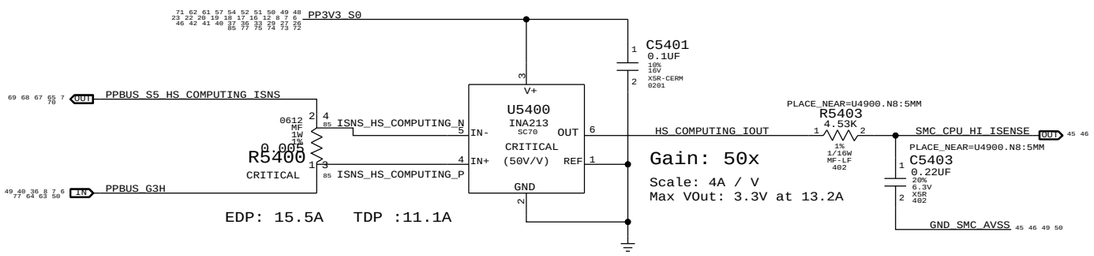
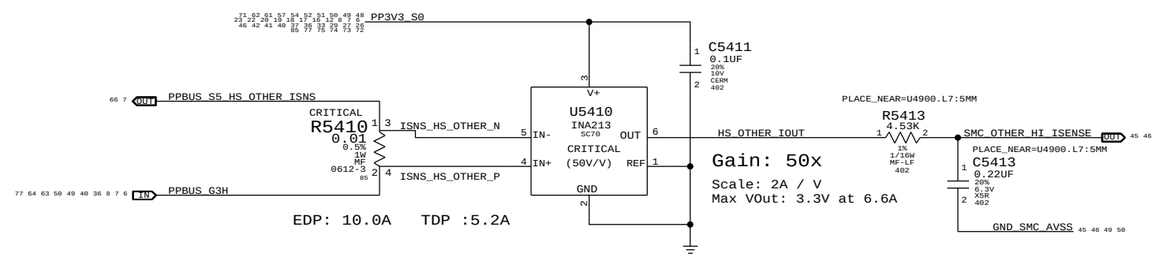
COMPUTING High Side Current Sense / Filter



Gain: 50x
Scale: 4A / V
Max VOut: 3.3V at 13.2A

EDP: 15.5A TDP :11.1A

OTHER High Side Current Sense / Filter

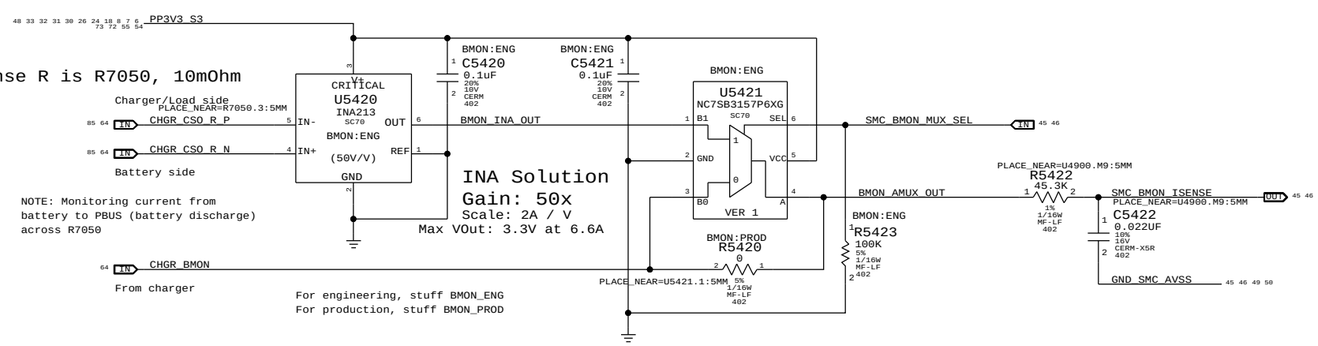


Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

EDP: 10.0A TDP :5.2A

CHARGER BMON High Side (BATTERY DISCHAEGE) Current Sense, MUX & Filter

Sense R is R7050, 10mOhm



NOTE: Monitoring current from battery to PBUS (battery discharge) across R7050

For engineering, stuff BMON_ENG
For production, stuff BMON_PROD

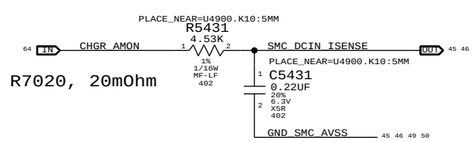
INA Solution
Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

INA (Engineering) Solution
Gain: 50x
Scale: 2A / V
Max VOut: 3.3V at 6.6A

Charger BMON (Production) Solution
ISL6259 Gain: 36x
Scale: 2.78A / V
Max VOut: 3.3V at 9.167A

DC-IN (AMON) Current Sense Filter

Sense R is R7020, 20mOhm



DC-In AMON
ISL6259 Gain: 20x
Scale: 2.5A / V
Max VOut: 3.3V at 8.25A

SYNC_MASTER=LINDA_K90I SYNC_DATE=10/22/2010

PAGE TITLE
High Side Current Sensing

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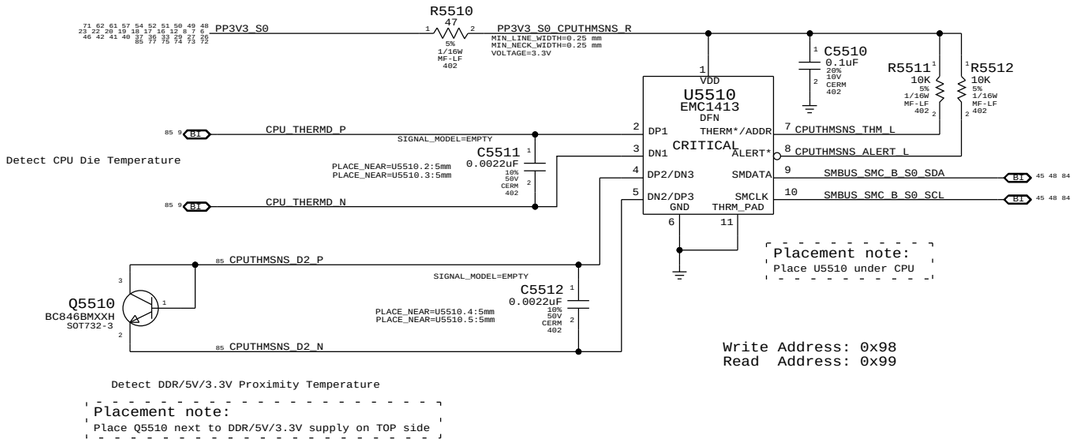
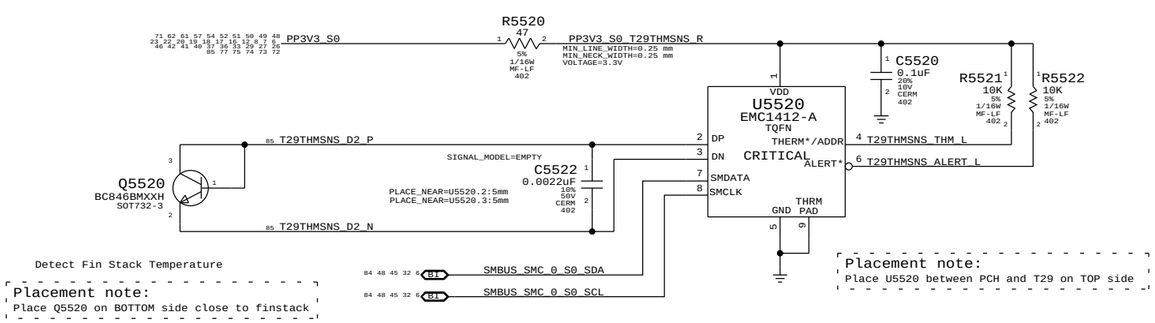
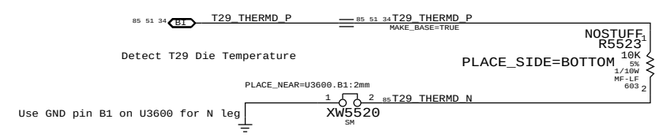
CPU Proximity/CPU Die/5V-3.3V Proximity



PCH-T29 Proximity/FinStack



T29 Die



SYNC_MASTER=LINDA_K90I	SYNC_DATE=10/22/2010
PAGE TITLE: Thermal Sensors	
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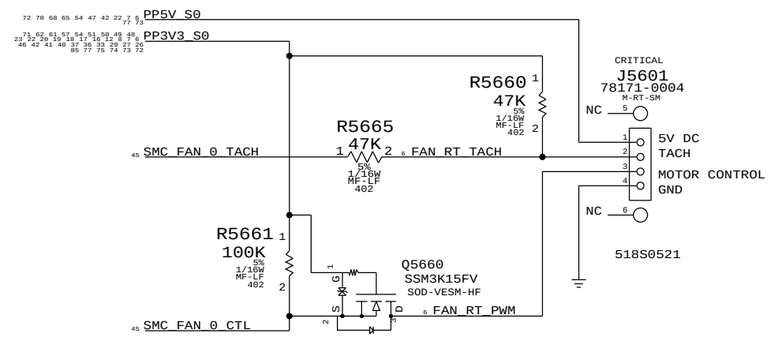

SYNC_MASTER=K24_MLB SYNC_DATE=07/20/2009

PAGE TITLE

Fan

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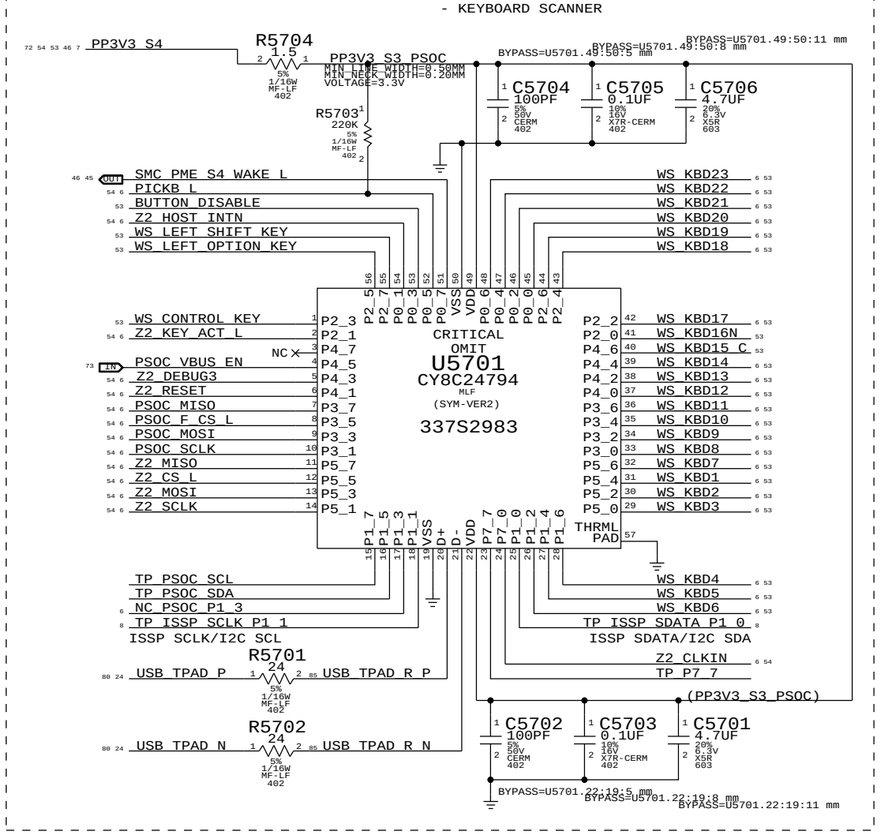
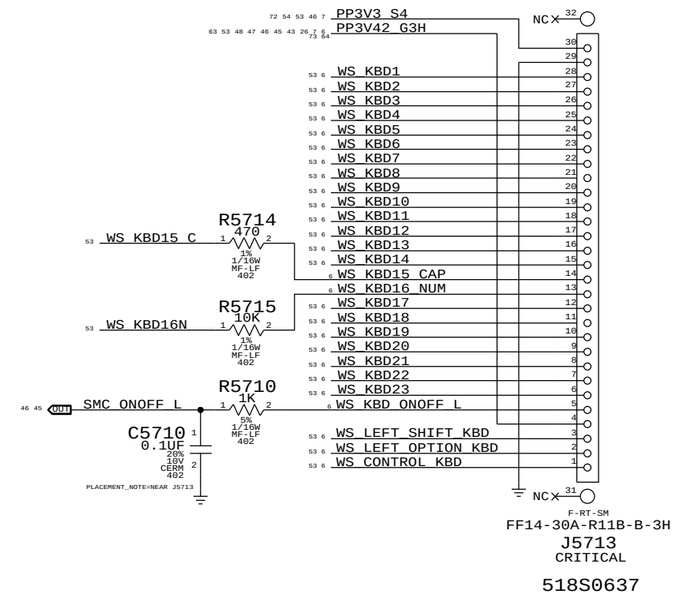
PSOC USB CONTROLLER

- USB INTERFACES TO MLB
- SPI HOST TO Z2
- TRACKPAD PICK BUTTONS
- KEYBOARD SCANNER



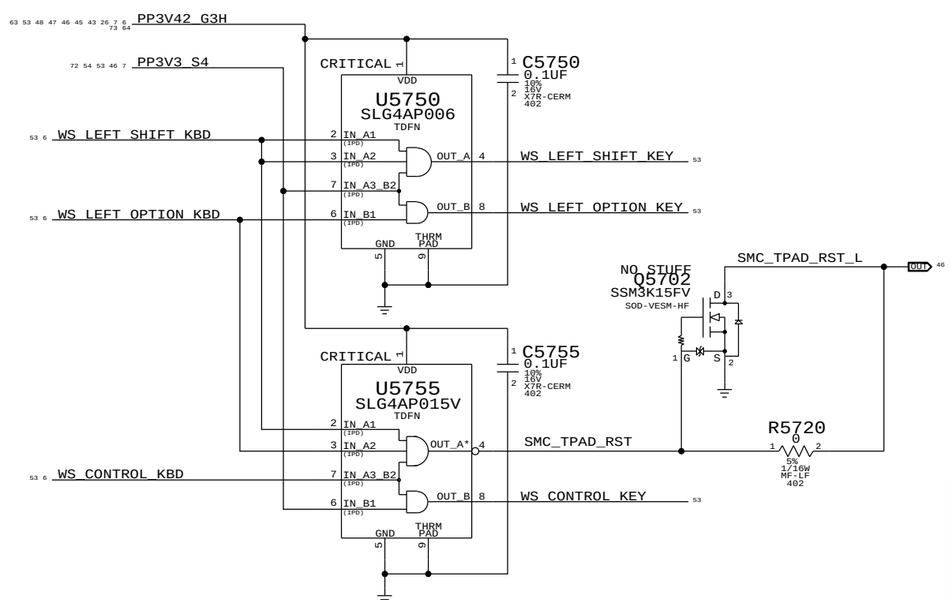
IC	PIN NAME	CURRENT	R_SNS	V_SNS	POWER
TMP102	V+	10UA 80UA	2.55 KOHM	0.0255 V 0.204 V	0.255E-6 W 16.32E-6 W
3V3 LDO	VDD VOUT	60MA (MAX) 60MA (MAX)	10 OHM 0.2 OHM	0.6 V 0.012 V	36E-3 W 0.72E-3 W
PSOC	VDD	8MA (TYP) 14MA (MAX)	1.5 OHM	0.012 V 0.021 V	96E-6 W 294E-6 W
18V BOOSTER	VIN	4MA (MAX)	4.7 OHM	0.0188 V	75.2E-6 W

Keyboard Connector

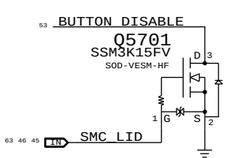


SMC Manual Reset & Isolation

Left shift, option & control keys combined with power button cause SMC RESET# assertion.
Keys ANDed with PSOC power to isolate when PSOC is not powered.



TPAD Buttons Disable



PLACE THESE COMPONENTS CLOSE TO J5800
THIS ASSUMES THERE'S A PP3V42_G3H PULL UP ON MLB

THE TPAD BUTTONS WILL BE DISABLE
WHEN THE LID IS CLOSED
LID OPEN => SMC_LID_LC ~ 3.42V
LID CLOSE => SMC_LID_LC < 0.50V

SYNC MASTER=LINDA K90I SYNC DATE=07/12/2010

PAGE TITLE
WELLSPRING 1

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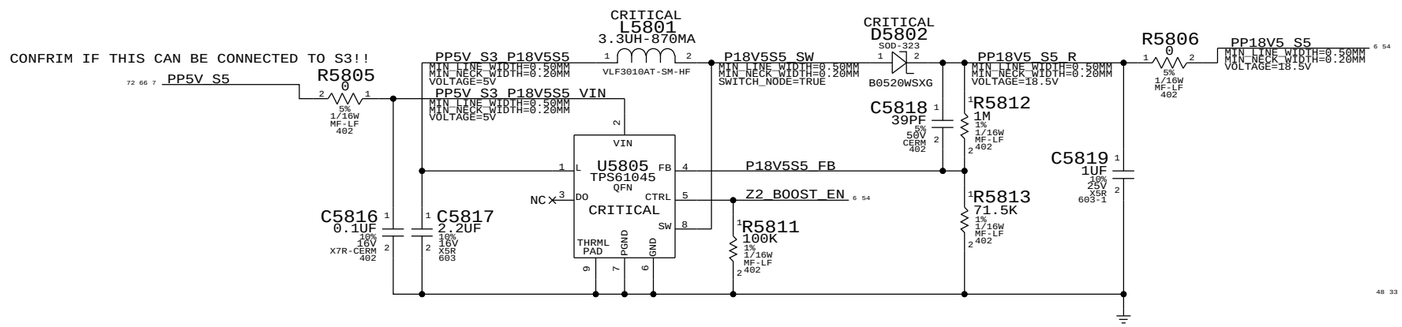
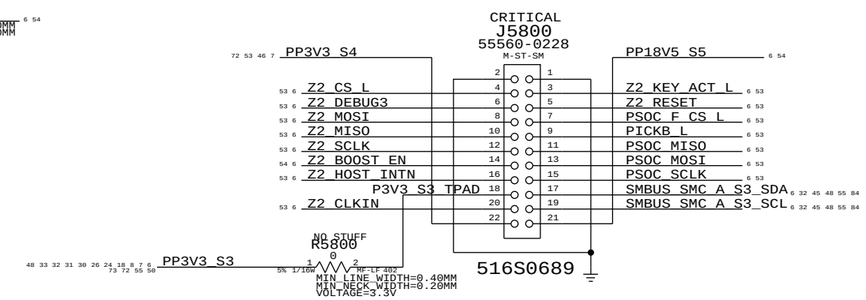
BOOSTER +18.5VDC FOR SENSORS

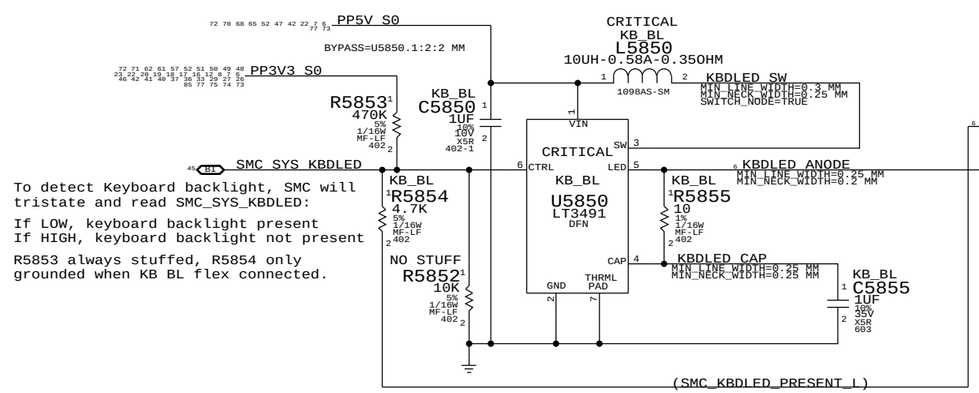
BOOSTER DESIGN CONSIDERATION:
- POWER CONSUMPTION
- DROOP LINE REGULATION
- RIPPLE TO MEET ERS
- 100-300 KHZ CLEAN SPECTRUM
- STARTUP TIME LESS THAN 2MS
- R5812,R5813,C5818 MODIFIED



IPD Flex Connector



Keyboard Backlight Driver & Detection

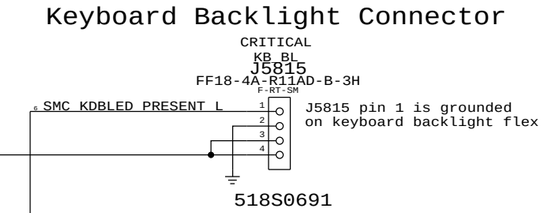


To detect Keyboard backlight, SMC will tristate and read SMC_SYS_KBDLED:

If LOW, keyboard backlight present
If HIGH, keyboard backlight not present

R5853 always stuffed, R5854 only grounded when KB BL flex connected.

Keyboard Backlight Connector



K6 NOTES : C5850 HAS BYPASS PROPERTY, SHOULD BE ADDED INCASE THIS PAGE IS SYNC'ED FROM T27

SYNC_MASTER=LINDA_K90I SYNC_DATE=07/12/2010

PAGE TITLE: WELLSPRING 2

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DRAWING NUMBER | SIZE: D

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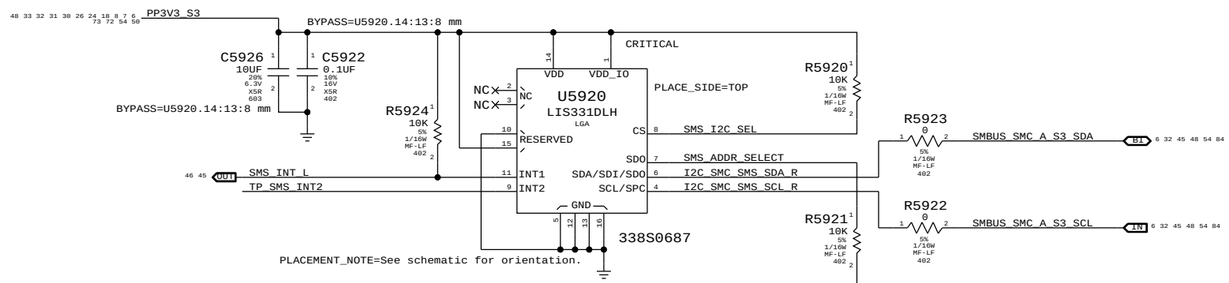
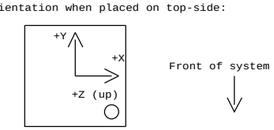


PLACEMENT_NOTE=See schematic for orientation.

SMS_ADDR_SELECT=0 Addr: 0x30(Wr)/0x31(Rd)
SMS_ADDR_SELECT=1 Addr: 0x32(Wr)/0x33(Rd)

NOTE: SDA and SCL have internal pull-ups to VDD_IO.

Desired orientation when placed on top-side:



Circle indicates pin 1 location when placed in correct orientation

SYNC_MASTER=LINDA K90I SYNC_DATE=07/08/2010

PAGE TITLE
Digital Accelerometer

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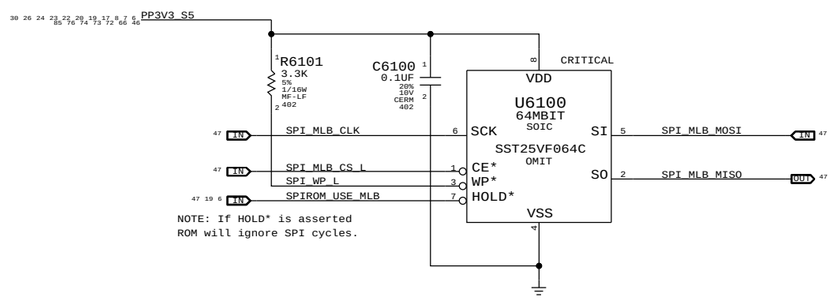

SYNC MASTER=K91_MLB SYNC DATE=05/15/2010

PAGE TITLE

SPI ROM

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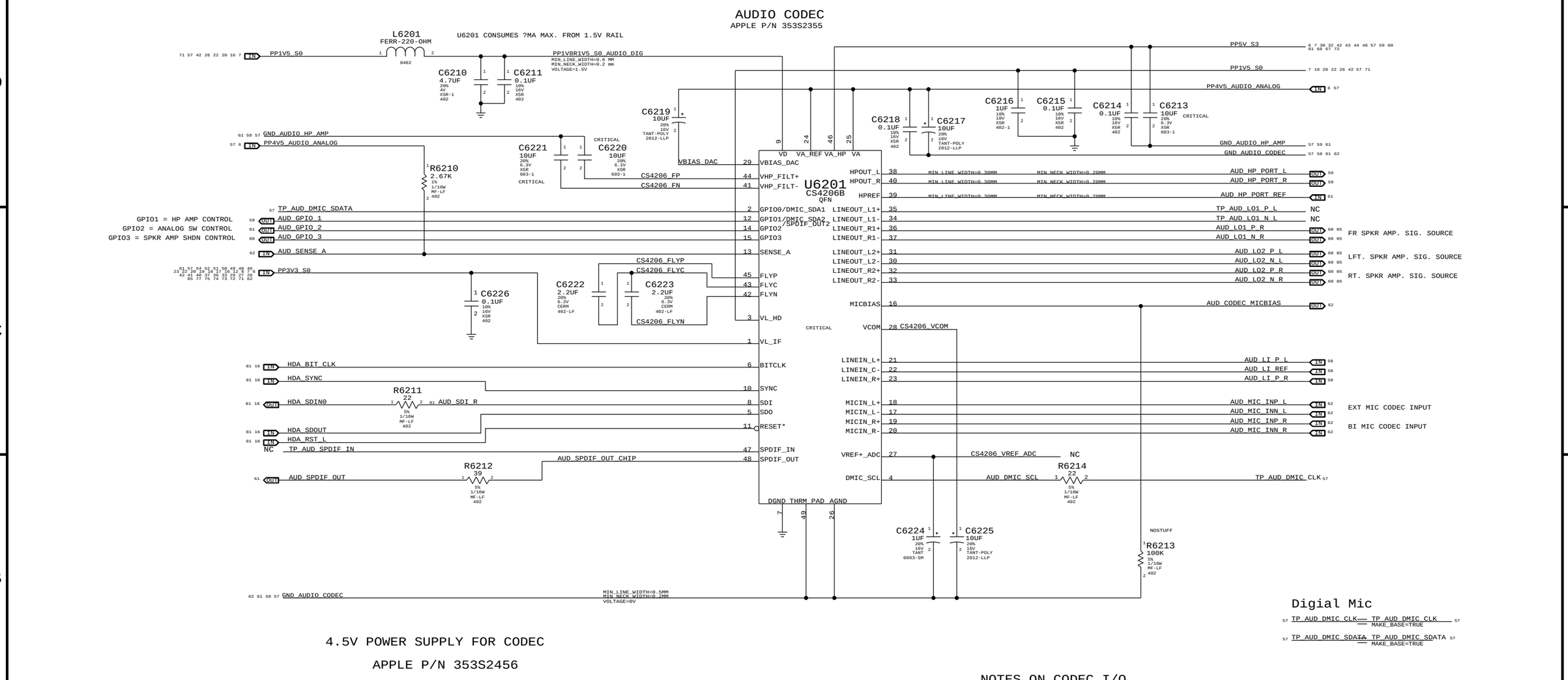

NOTES ON CODEC I/O

DIFF FSINPUT= 2.45VRMS
SE FSINPUT= 1.22VRMS
DAC1 FSOUTPUT= 1.34VRMS
DAC2/3 FSOUTPUTDIFF= 2.67VRMS
DAC2/3 FSOUTPUTSE= 1.34VRMS

SYNC_MASTER=LENG_K90I SYNC_DATE=08/10/2010

PAGE TITLE
AUDIO: CODEC/REGULATOR

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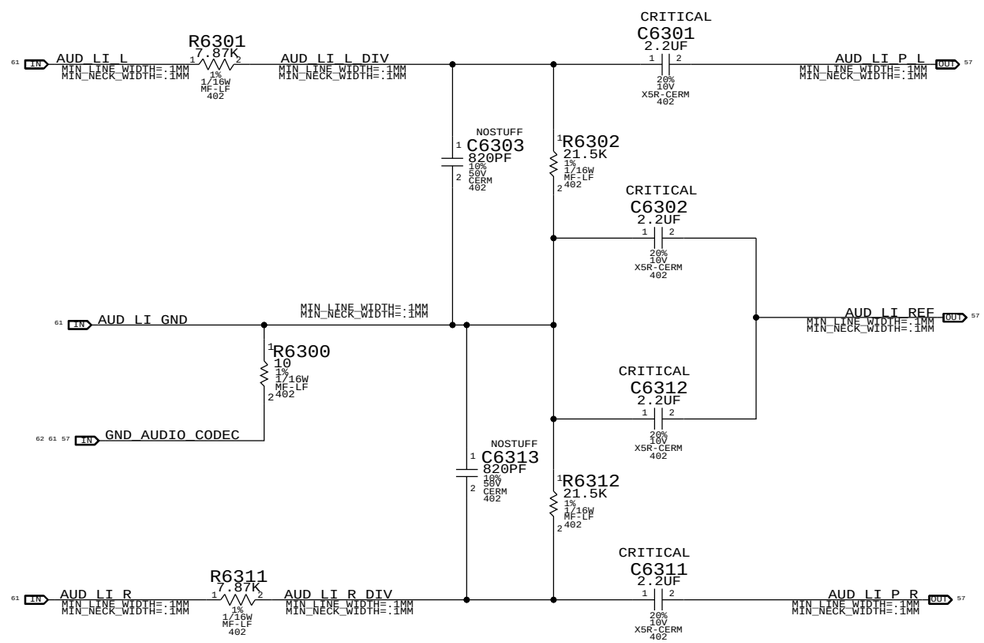
LINE INPUT VOLTAGE DIVIDER

CODEC RIN = 20K OHMS
NET RIN = 10.36K OHMS (INCLUDING PULL-DOWNS AT ANALOG SWITCH COM PINS)
FC_HP = 3.6 HZ
FC_LP = 43KHZ
VIN = 2VRMS, CODEC VIN = 1.14 VRMS



PAGE TITLE
AUDIO: LINE INPUT FILTER

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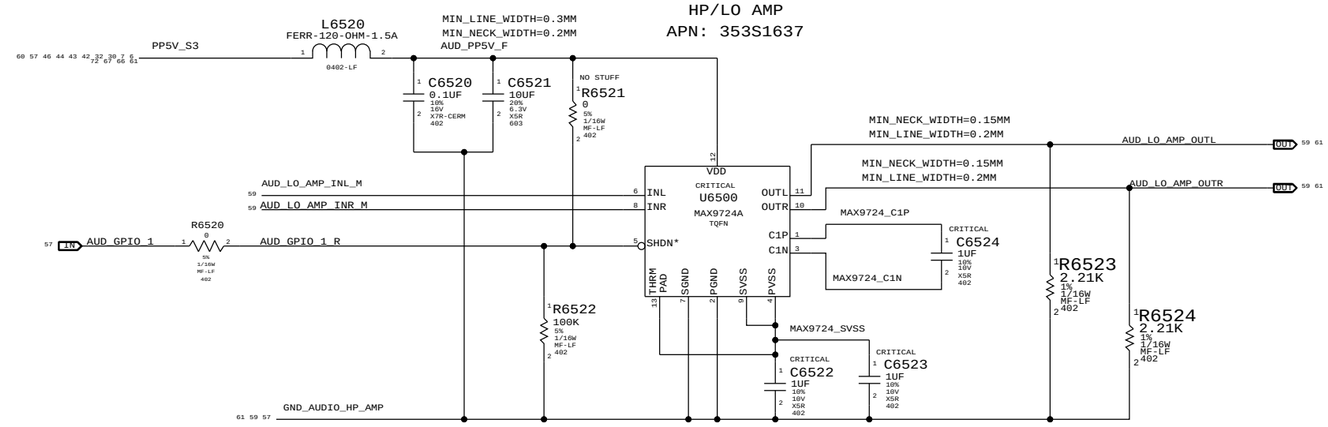
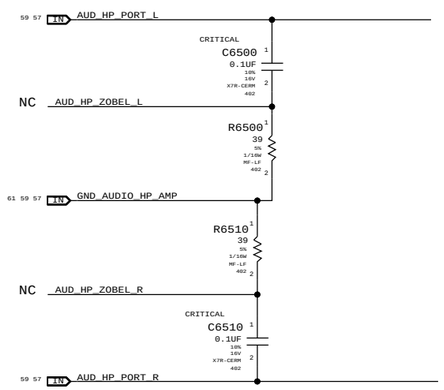
FOR PROTO2, STUFF R6521 AND NO STUFF R6520 AND R6522 UNTIL
RE-TASKABLE IO SW SUPPORT AVAILABLE (FORCES IO INTO OUTPUT MODE).

HP/LO AMP
APN: 353S1637

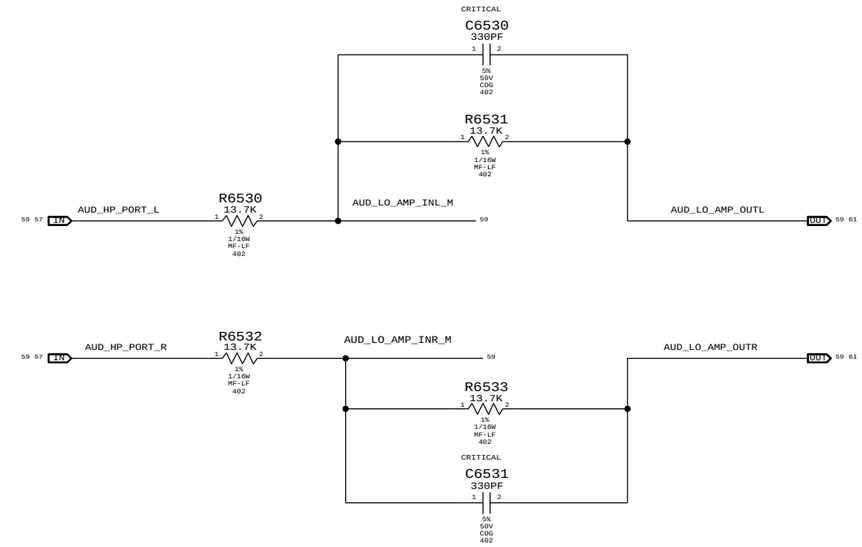


ZOBEL NETWORK & 1ST ORDER DAC FILTER PLACEHOLDER



MAX9724 GAIN/FILTER COMPONENTS

AV_PB = -1V/V, FC_LPF = 35.2KHZ



SYNC_MASTER=LENG_K90I SYNC_DATE=08/10/2010

PAGE TITLE
AUDIO: HEADPHONE FILTER

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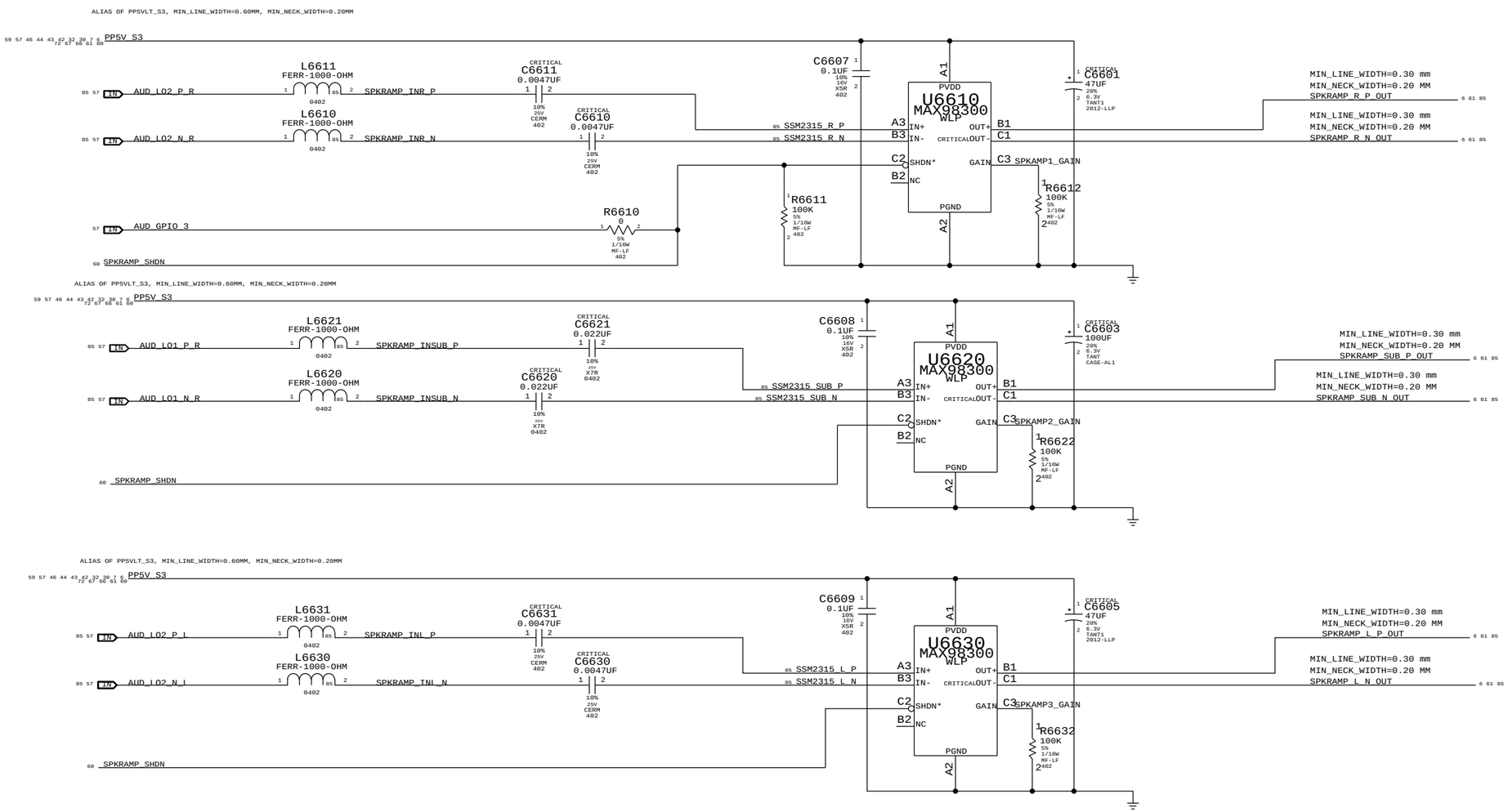
SATELLITE & SUB TWEETER AMPLIFIER

APN:353S2888

SATELLITE	169 HZ < FC < 282 HZ
SUB	80 HZ < FC < 132 HZ
GAIN	3DB



SYNC MASTER=LENG_K90I SYNC DATE=08/10/2010

PAGE TITLE

AUDI0: SPEAKER AMP

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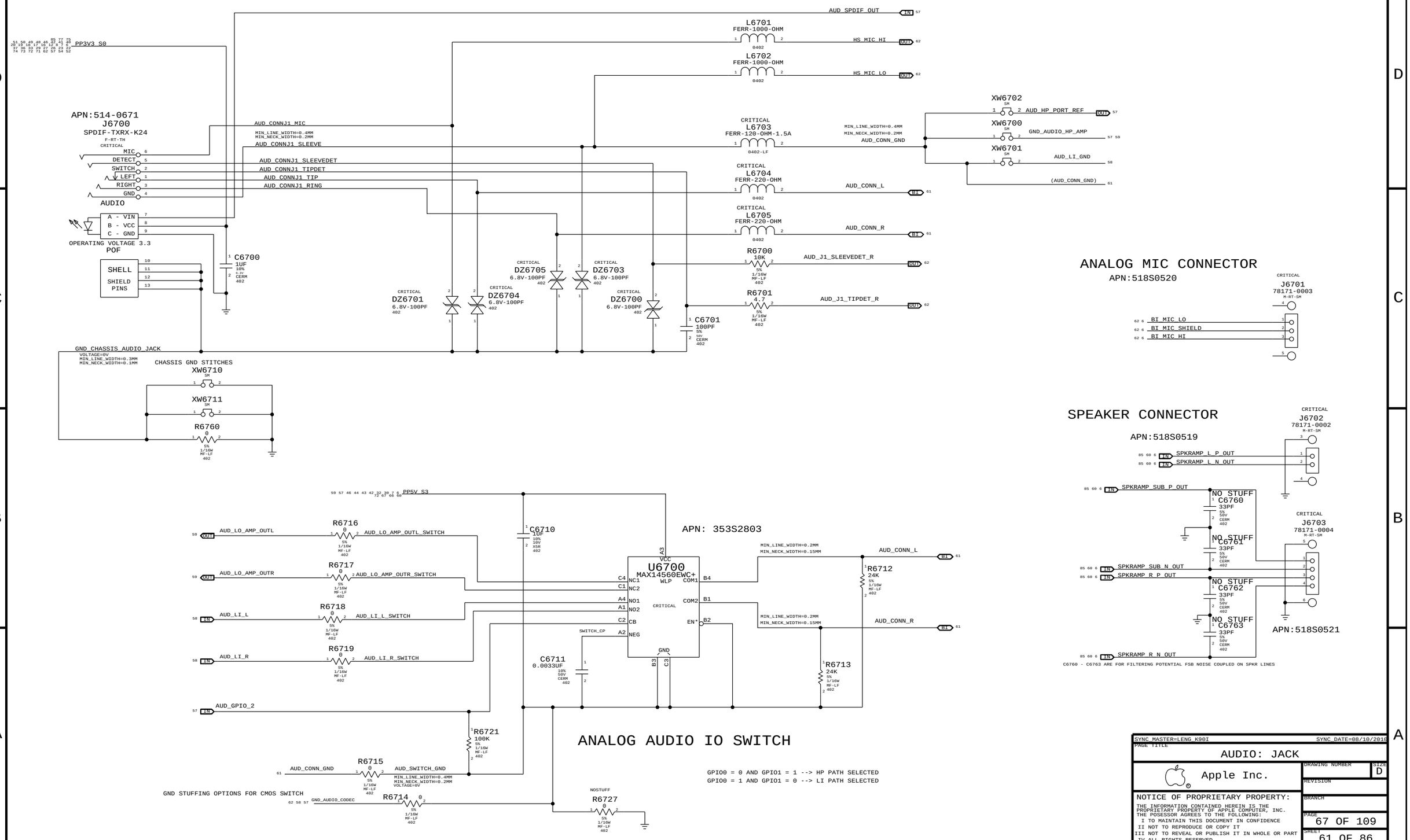
AUDIO JACK: LI/LO/HP CONNECTOR, SPDIF TX



SYNC_MASTER=LENG_K90I SYNC_DATE=08/10/2010

PAGE TITLE: AUDIO: JACK

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CODEC OUTPUT SIGNAL PATHS

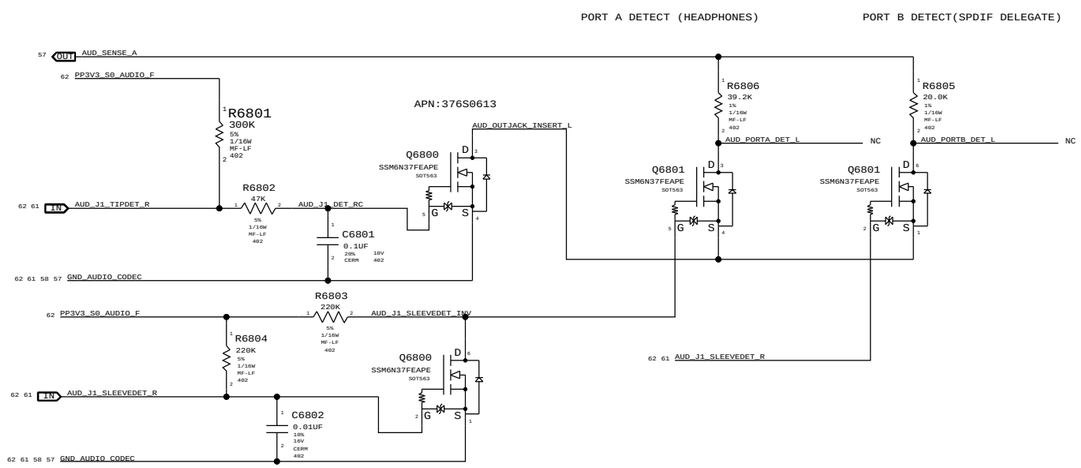
FUNCTION	VOLUME	CONVERTER	PIN COMPLEX	MUTE CONTROL	DET ASSIGNMENT
HP/LINE OUT	0X02 (2)	0X02 (2)	0X09 (9,A)	GPIO_2 AND GPIO_1	0X09 (A)
LINE IN	0X05 (5)	0X05 (5)	0X0C (12)	GPIO_2 AND GPIO_1	0X09 (A)AND UI ELEMENT
SATELLITES	0X04 (4)	0X04 (4)	0X0B (11)	GPIO_3	N/A
SUB	0X03 (3)	0X03 (03)	0X0A (10)	GPIO_3	N/A
SPDIF OUT	N/A	0X08 (8)	0X10 (16)	N/A	0X0D (B)

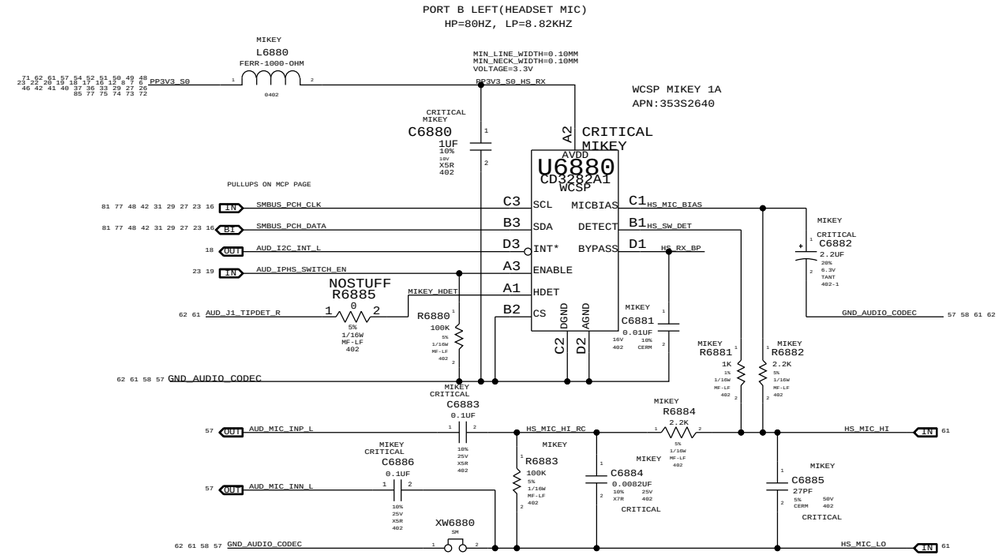
CODEC INPUT SIGNAL PATHS

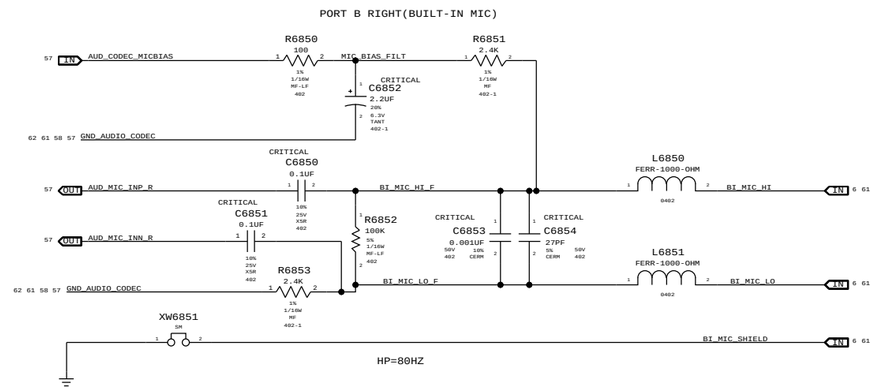
FUNCTION	CONVERTER	PIN COMPLEX	VREF	DET ASSIGNMENT
BUILT-IN MIC	0X06 (6)	0X0D (13,B,RIGHT)	MIC_BIAS (80%)	N/A
HEADSET MIC	0X06 (6)	0X0D (13,V22,B,LEFT)	MIKEY	MIKEY

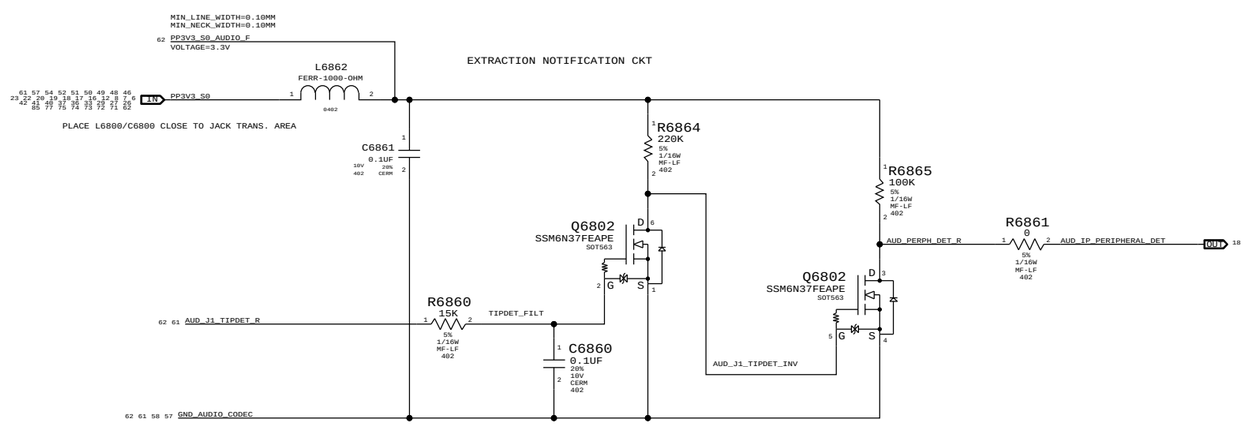
SOUTHBRIDGE RESOURCES

FUNCTION	SYSTEM GPIO	SYSTEM INTERRUPT
AUD_IPHS_SWITCH_EN	COUGAR_POINT GPIO16	N/A
AUD_I2C_INT_L	N/A	COUGAR_POINT GPIO5/PIRQH
AUD_IP_PERIPHERAL_DET	N/A	COUGAR_POINT GPIO3/PIRQH









SYNC MASTER=LENG K90I SYNC DATE=08/10/2010

PAGE TITLE

AUDIO: JACK TRANSLATORS

Apple Inc.

DRAWING NUMBER

SIZE D

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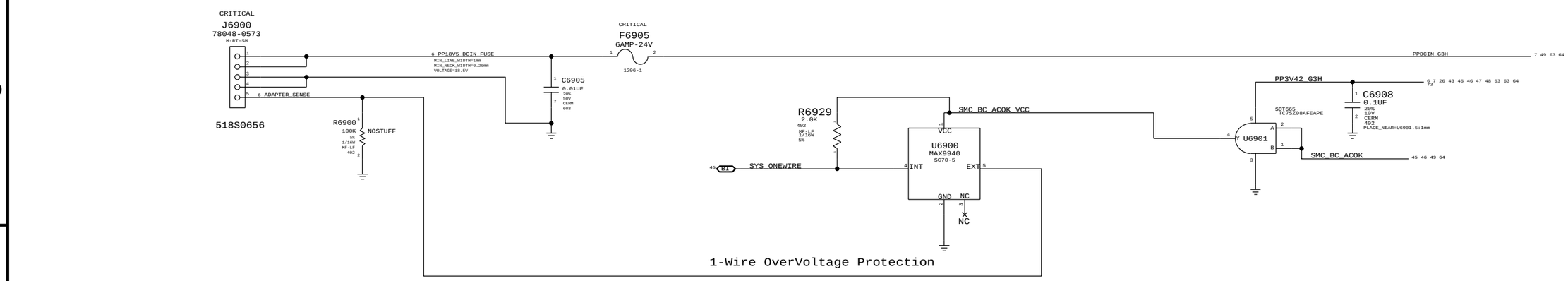
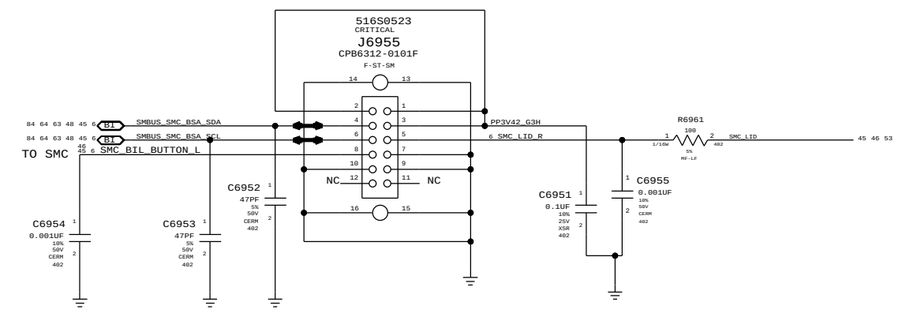
MagSafe DC Power Jack

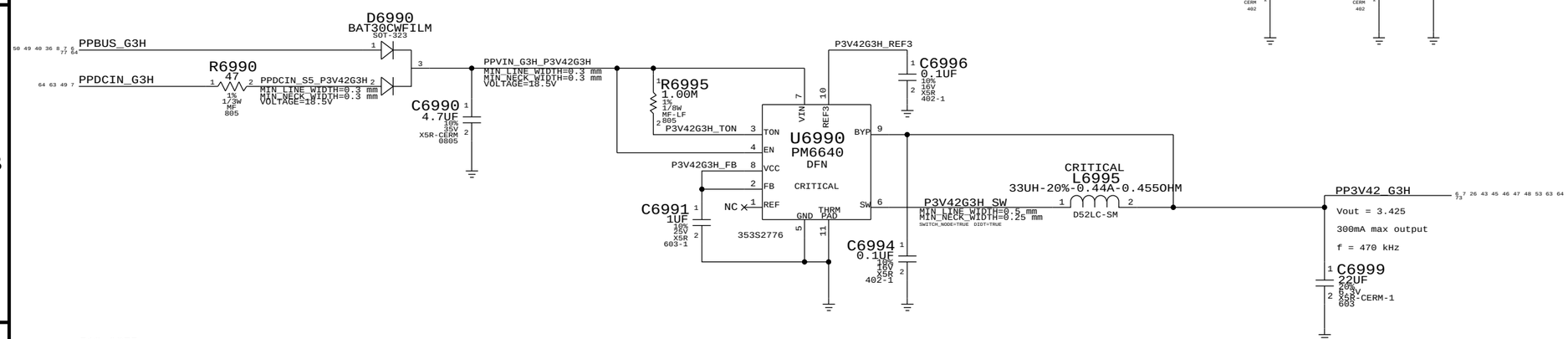


BIL CONNECTOR

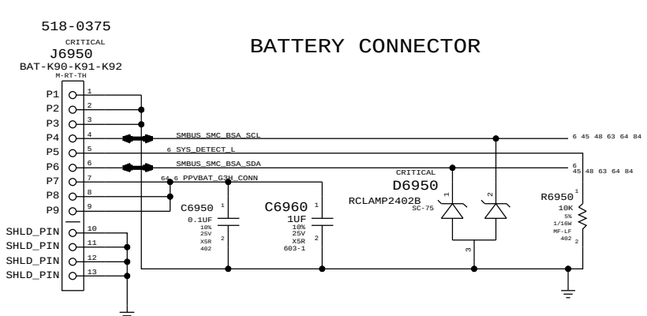


3.425V "G3Hot" Supply

Supply needs to guarantee 3.31V delivered to SMC VRef generator



BATTERY CONNECTOR



SYNC MASTER=JACK_K90I	SYNC DATE=08/20/2010
PAGE TITLE: DC-In & Battery Connectors	
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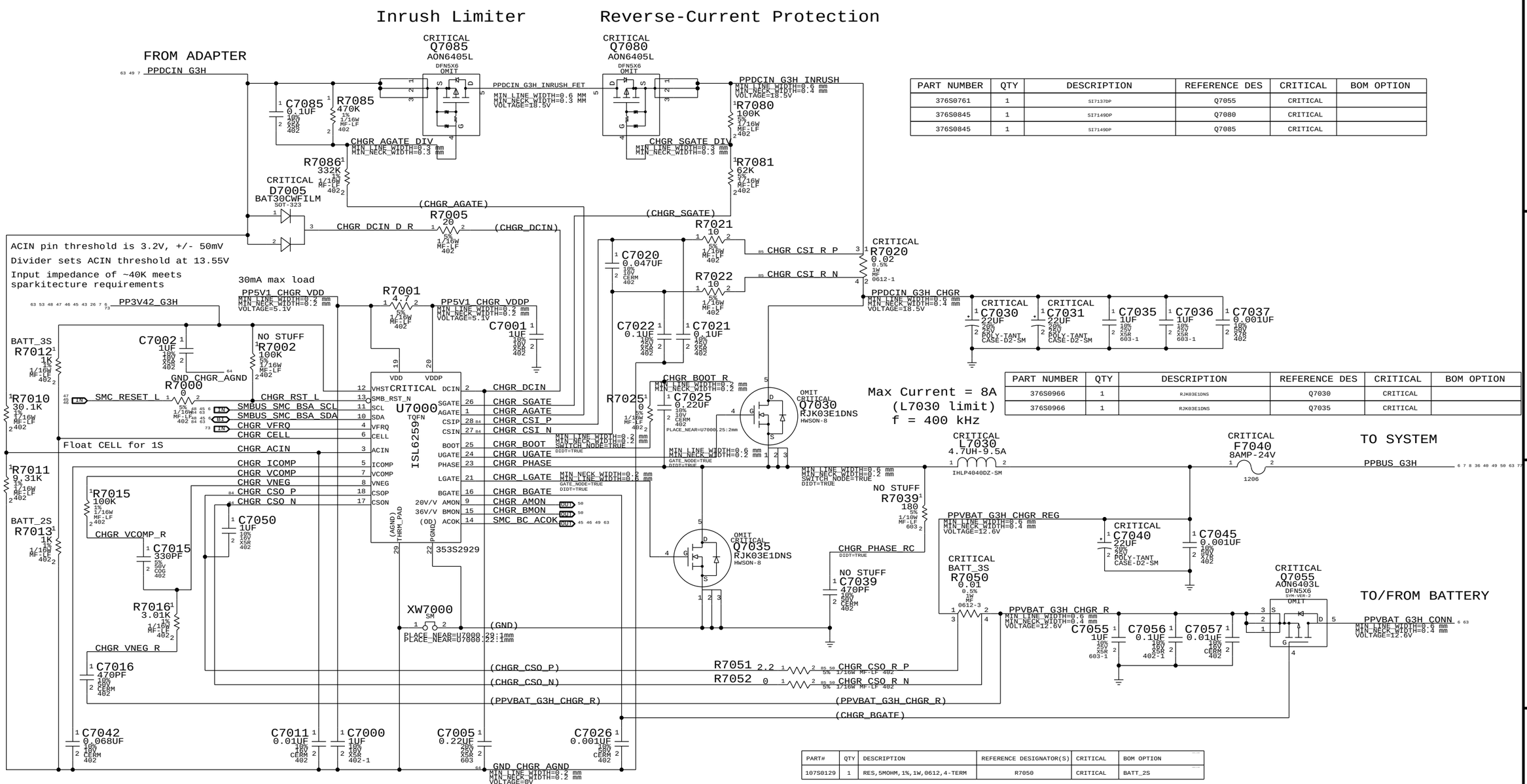

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0761	1	SI7137DP	Q7055	CRITICAL	
376S0845	1	SI7149DP	Q7080	CRITICAL	
376S0845	1	SI7149DP	Q7085	CRITICAL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7030	CRITICAL	
376S0966	1	RJK03E1DNS	Q7035	CRITICAL	

PART#	QTY	DESCRIPTION	REFERENCE DESIGNATOR(S)	CRITICAL	BOM OPTION
107S0129	1	RES,5MOHM,1%,1W,0612,4-TERM	R7050	CRITICAL	BATT_2S

K6 NOTES : L7030 CHANGED BACK TO K24 IND DUE TO LAYOUT

SYNC MASTER=JACK K90I SYNC DATE=10/11/2010

PAGE TITLE: PBus Supply & Battery Charger

Apple Inc.

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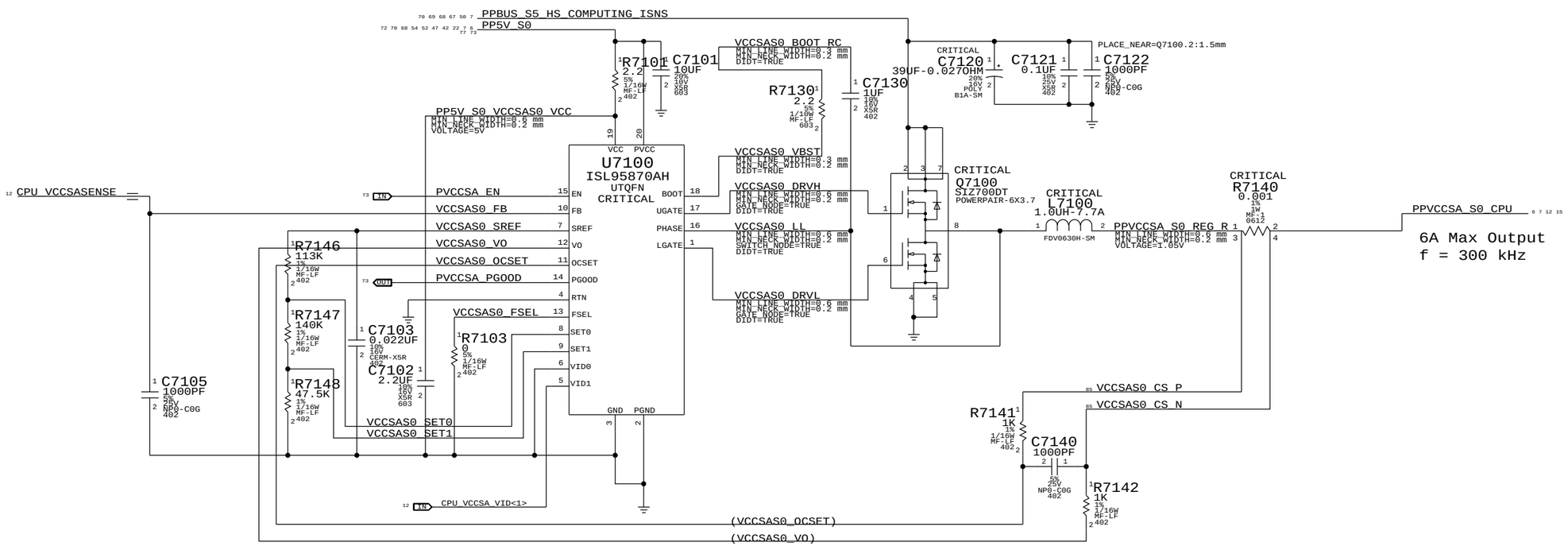
System Agent Power Supply



SYNC MASTER=JACK K90I SYNC DATE=08/19/2010

PAGE TITLE
System Agent Supply

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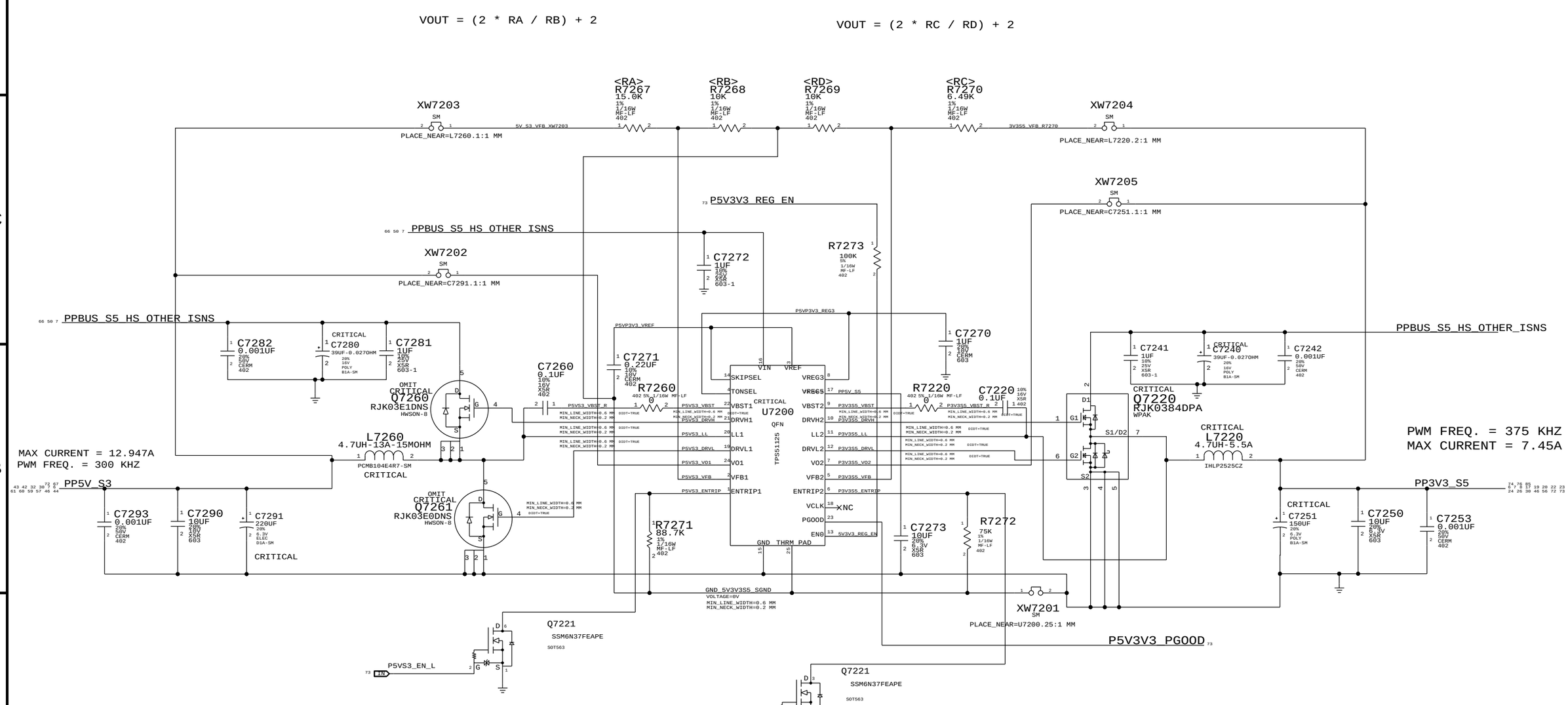
5V_S3/3.3V_S5 POWER SUPPLY



PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0966	1	RJK03E1DNS	Q7260	CRITICAL	
376S0895	1	RJK03E0DNS	Q7261	CRITICAL	

SYNC MASTER=JACK K90I SYNC DATE=10/04/2010

PAGE TITLE: 5V/3.3V SUPPLY

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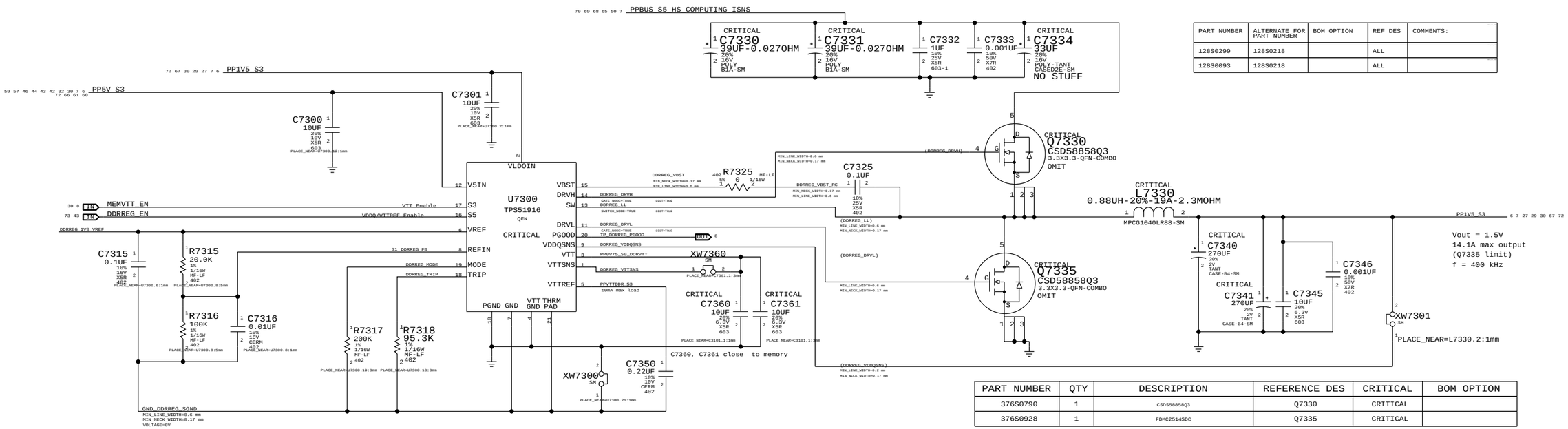

PART NUMBER	ALTERNATE FOR PART NUMBER	BOM OPTION	REF DES	COMMENTS:
128S0299	128S0218		ALL	
128S0093	128S0218		ALL	

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
376S0790	1	CSD55885Q3	Q7330	CRITICAL	
376S0928	1	FDMC2514SDC	Q7335	CRITICAL	

SYNC_MASTER=JACK_K90I SYNC_DATE=10/11/2010

PAGE TITLE

1.5V DDR3 Supply

Apple Inc.

DRAWING NUMBER

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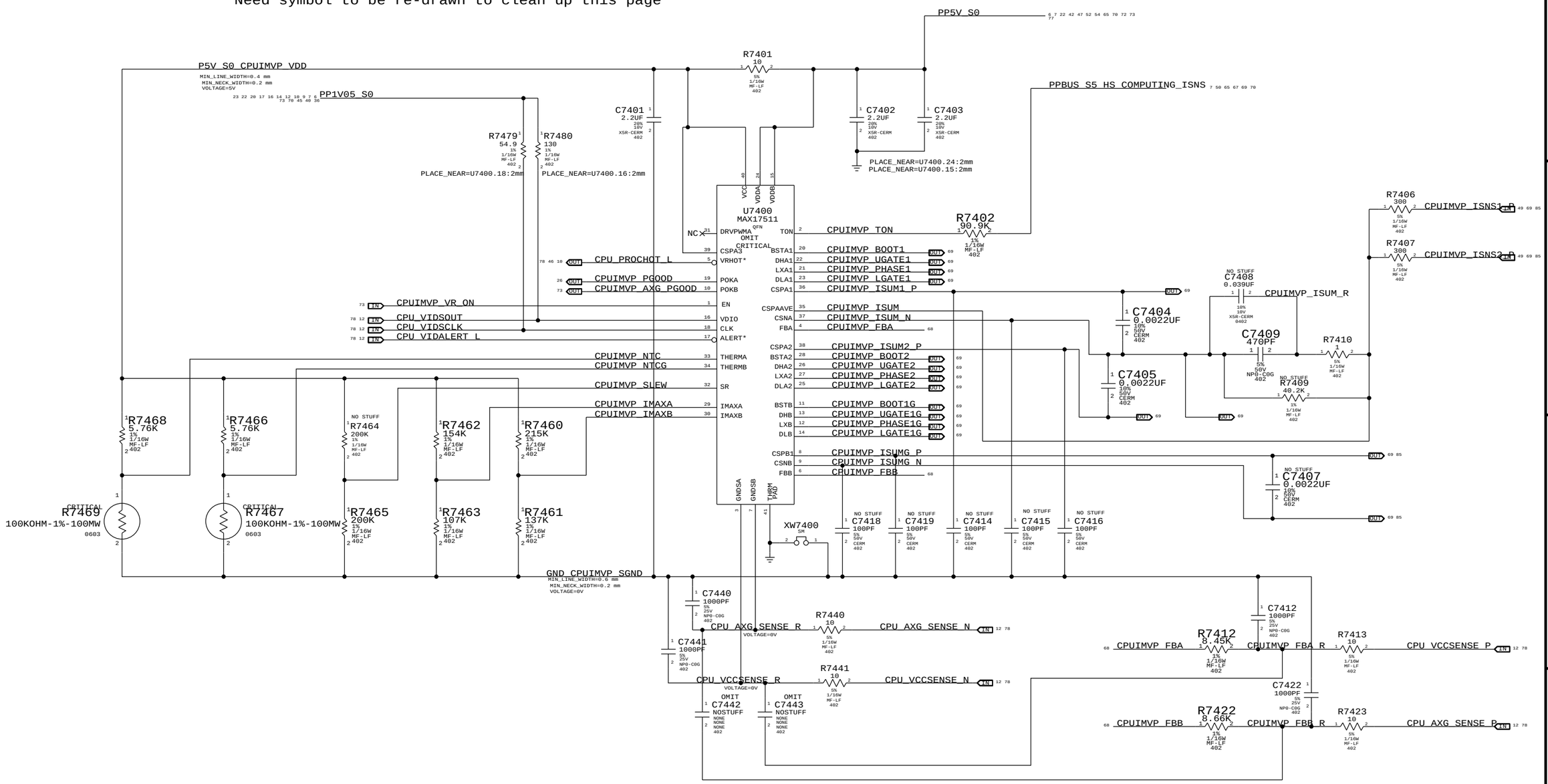
PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
353S3259	1	IC,MAX15092,3+1PH CPU REG,IMVP7,5X5QFN40	U7400	CRITICAL	

Need symbol to be re-drawn to clean up this page



SYNC_MASTER=JACK_K99I SYNC_DATE=10/14/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Regulator

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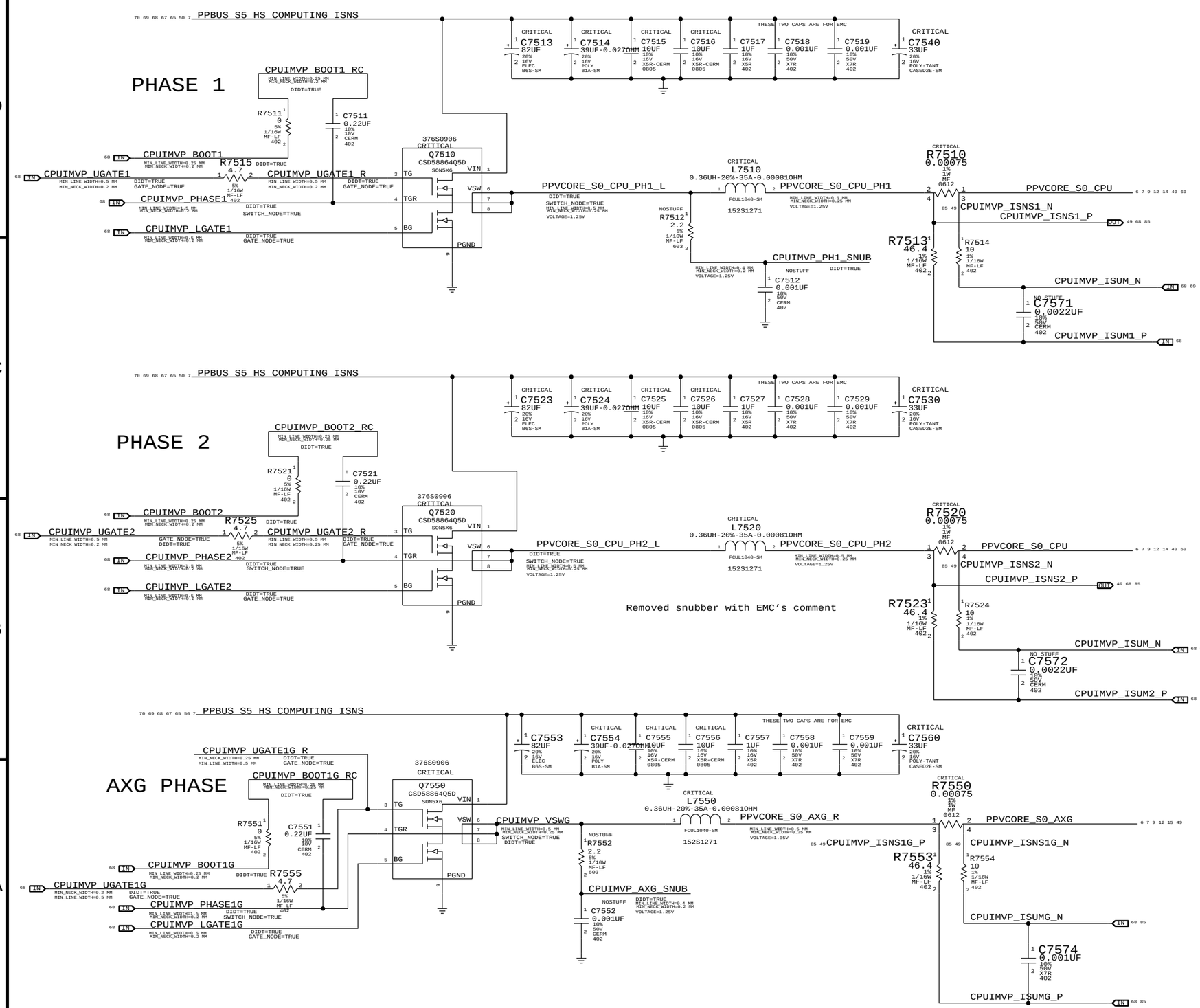

SYNC_MASTER=JACK_K901 SYNC_DATE=09/03/2010

PAGE TITLE

CPU IMVP7 & AXG VCore Output

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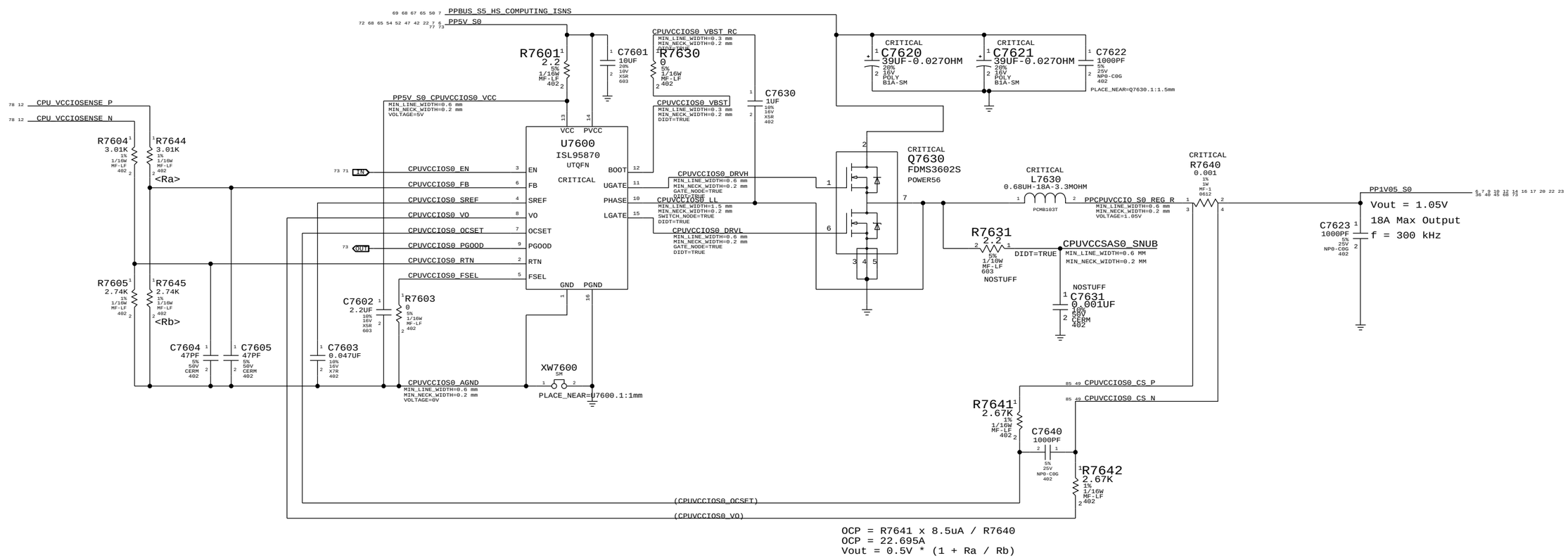
CPU VCCIO (1.05V S0) Regulator



SYNC_MASTER=JACK K90I SYNC_DATE=08/19/2010

PAGE TITLE
CPUVCCIO (1.05V) Power Supply

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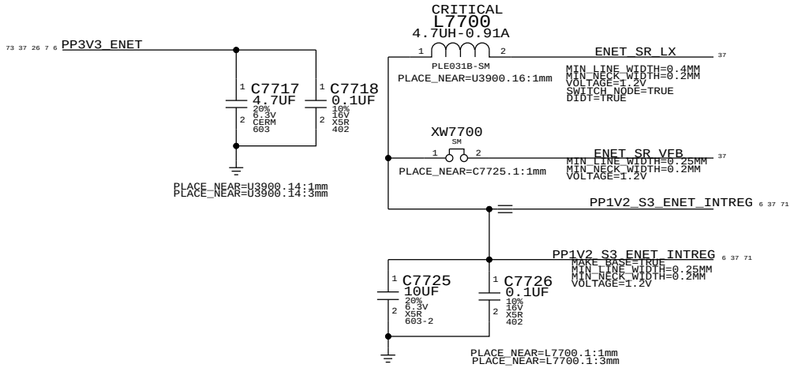
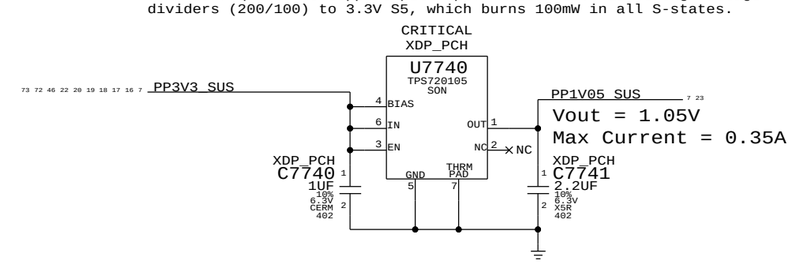
CAESAR IV 1.2V INT.VR CMPTS



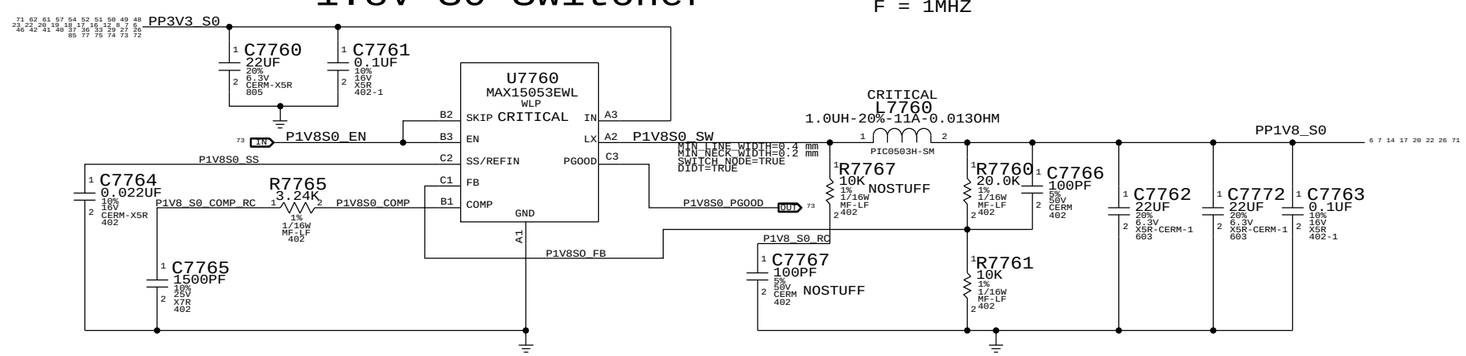
1.05V S5 LDO

Cougar Point requires JTAG pull-ups to be powered at 1.05V in S5.
Pull-ups (3) must be 51 ohms to support XDP (not required in production).
70mA is required to support pull-ups. Alternative is strong voltage
dividers (200/100) to 3.3V S5, which burns 100mW in all S-states.

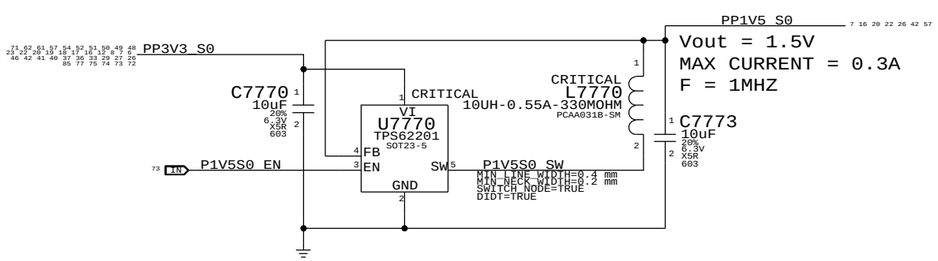


1.8V S0 Switcher

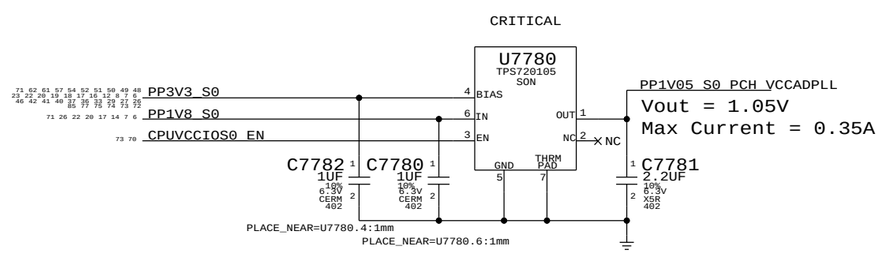
Vout = 1.8V
MAX CURRENT = 2A
F = 1MHZ



1.5V S0 Switcher



1.05V S0 LDO



SYNC MASTER=JACK K90I SYNC DATE=08/19/2010

PAGE TITLE
Misc Power Supplies

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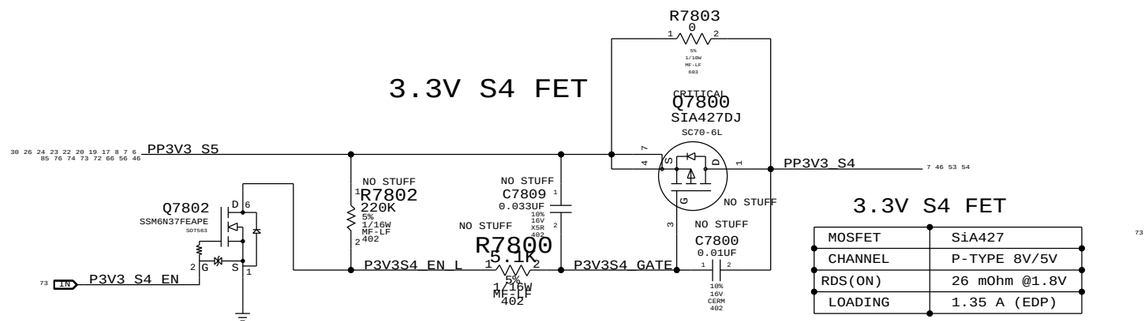
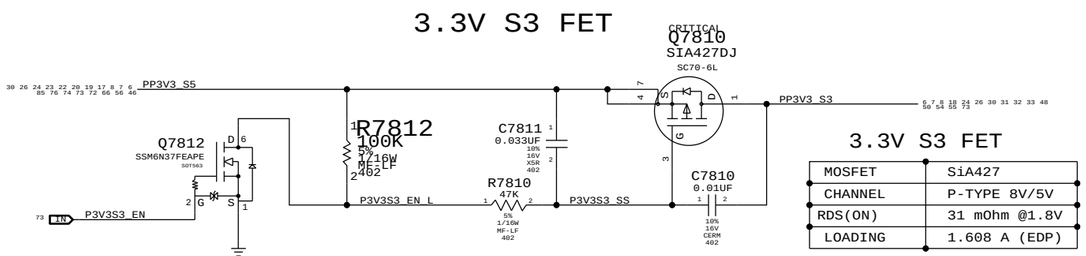


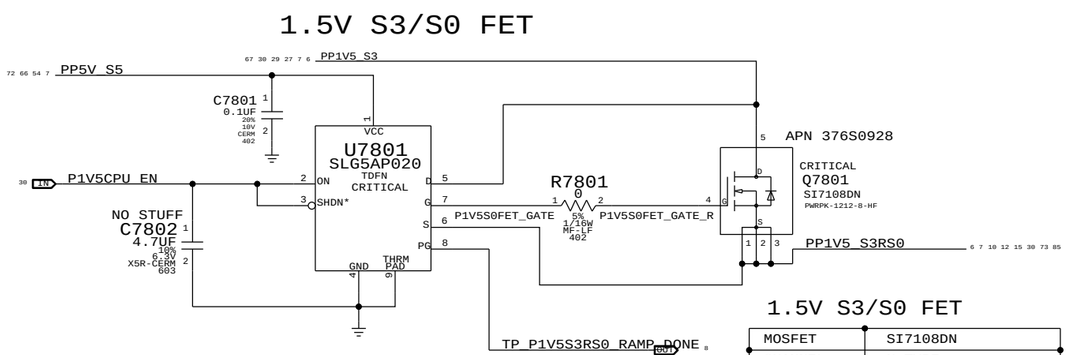
3.3V S4 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	1.35 A (EDP)



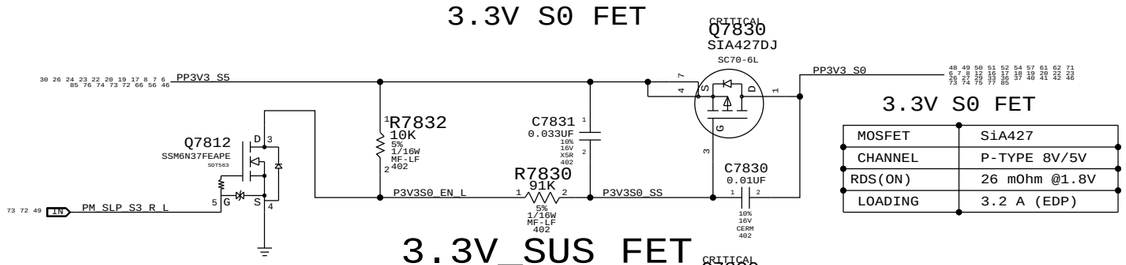
3.3V S3 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	31 mOhm @1.8V
LOADING	1.608 A (EDP)



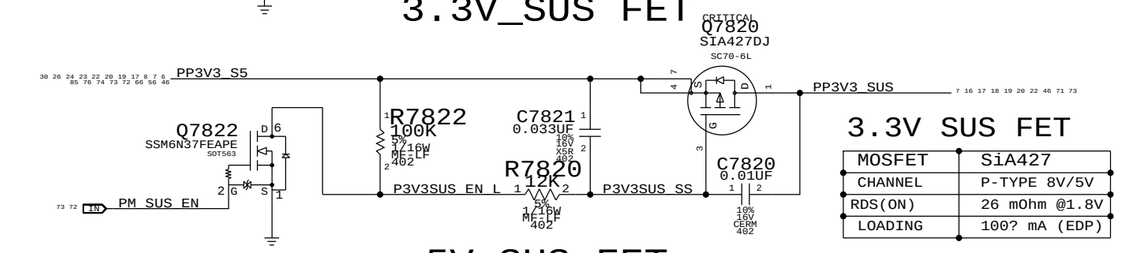
1.5V S3/S0 FET

MOSFET	SI7108DN
CHANNEL	N-TYPE
RDS(ON)	6 mOhm @4.5V
LOADING	5 A (EDP)



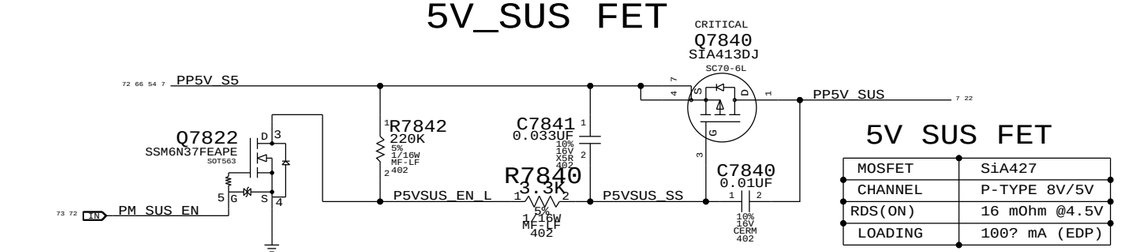
3.3V S0 FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	3.2 A (EDP)



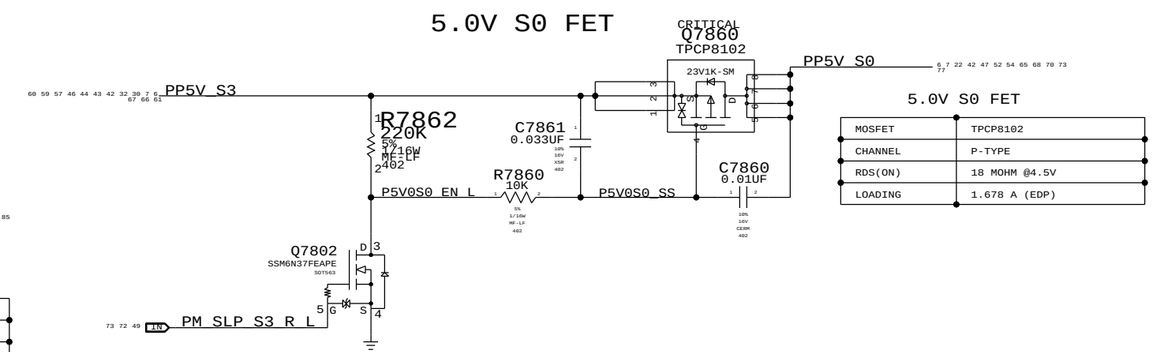
3.3V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	26 mOhm @1.8V
LOADING	100? mA (EDP)



5V SUS FET

MOSFET	SiA427
CHANNEL	P-TYPE 8V/5V
RDS(ON)	16 mOhm @4.5V
LOADING	100? mA (EDP)



5.0V S0 FET

MOSFET	TPCP8102
CHANNEL	P-TYPE
RDS(ON)	18 MOHM @4.5V
LOADING	1.678 A (EDP)

SYNC MASTER=JACK_K90I SYNC DATE=10/22/2010

PAGE TITLE: Power FETs

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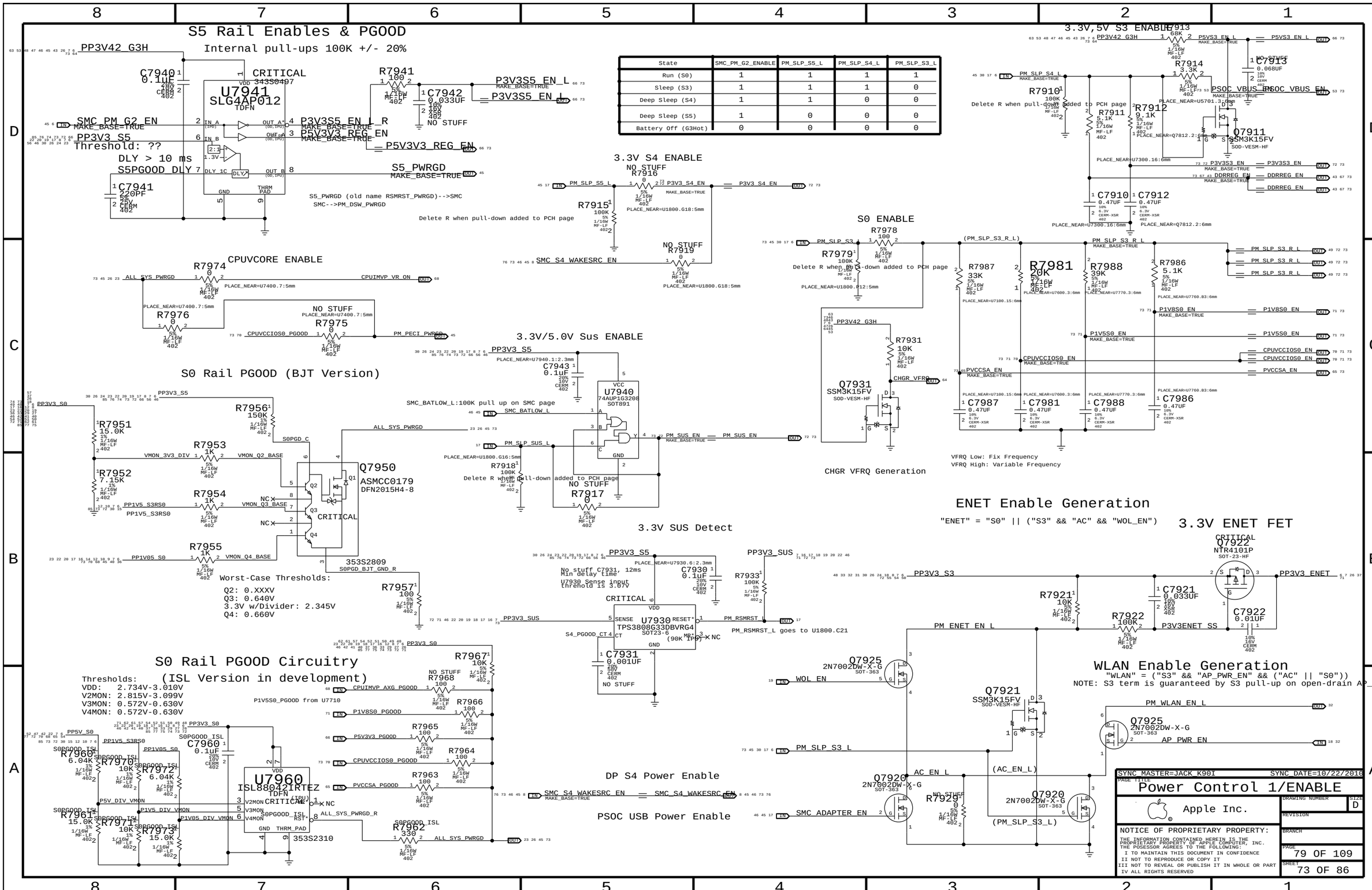

State	SMC_PM_G2_ENABLE	PM_SLP_S5_L	PM_SLP_S4_L	PM_SLP_S3_L
Run (S0)	1	1	1	1
Sleep (S3)	1	1	1	0
Deep Sleep (S4)	1	1	0	0
Deep Sleep (S5)	1	0	0	0
Battery Off (G3Hot)	0	0	0	0

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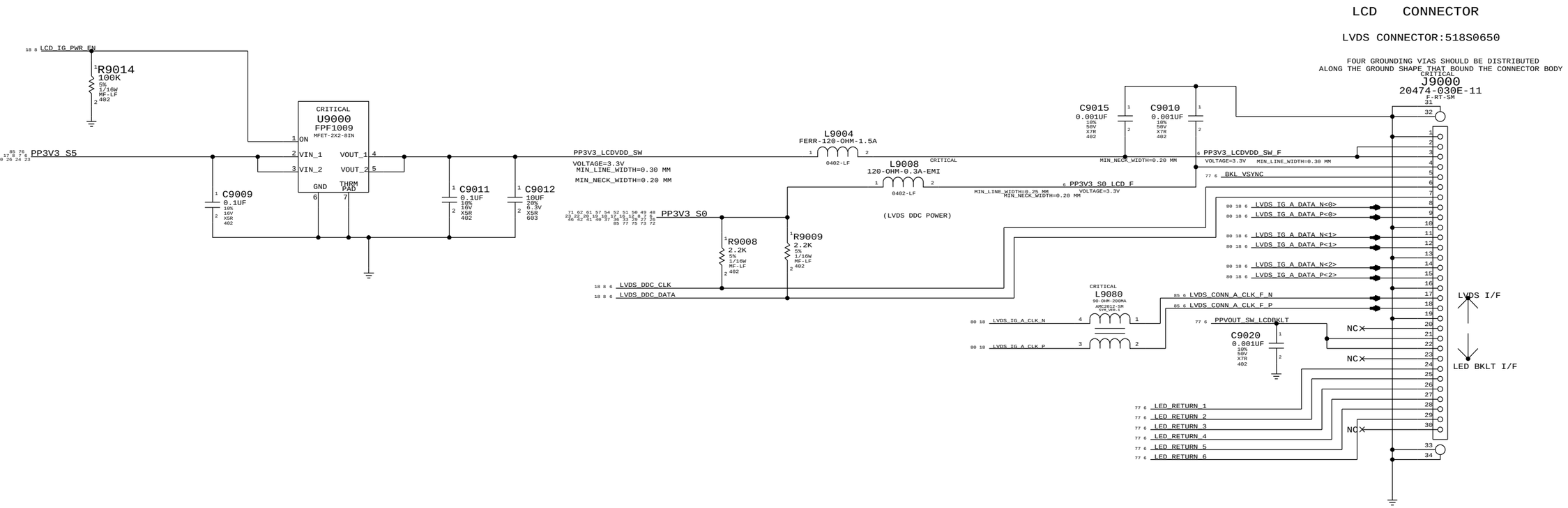

SYNC_MASTER=K24_MLB SYNC_DATE=07/20/2009

PAGE TITLE

LVDS CONNECTOR

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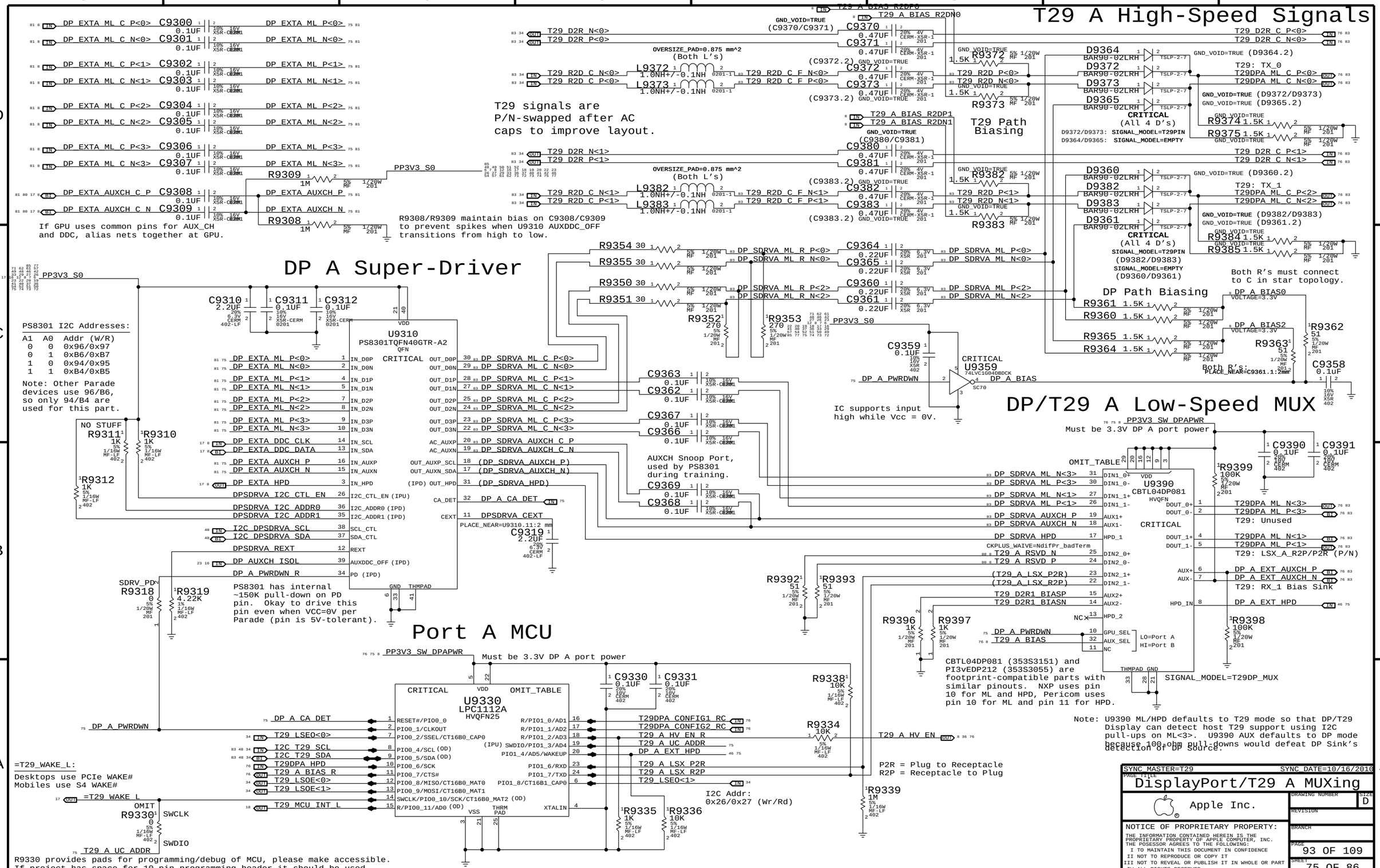

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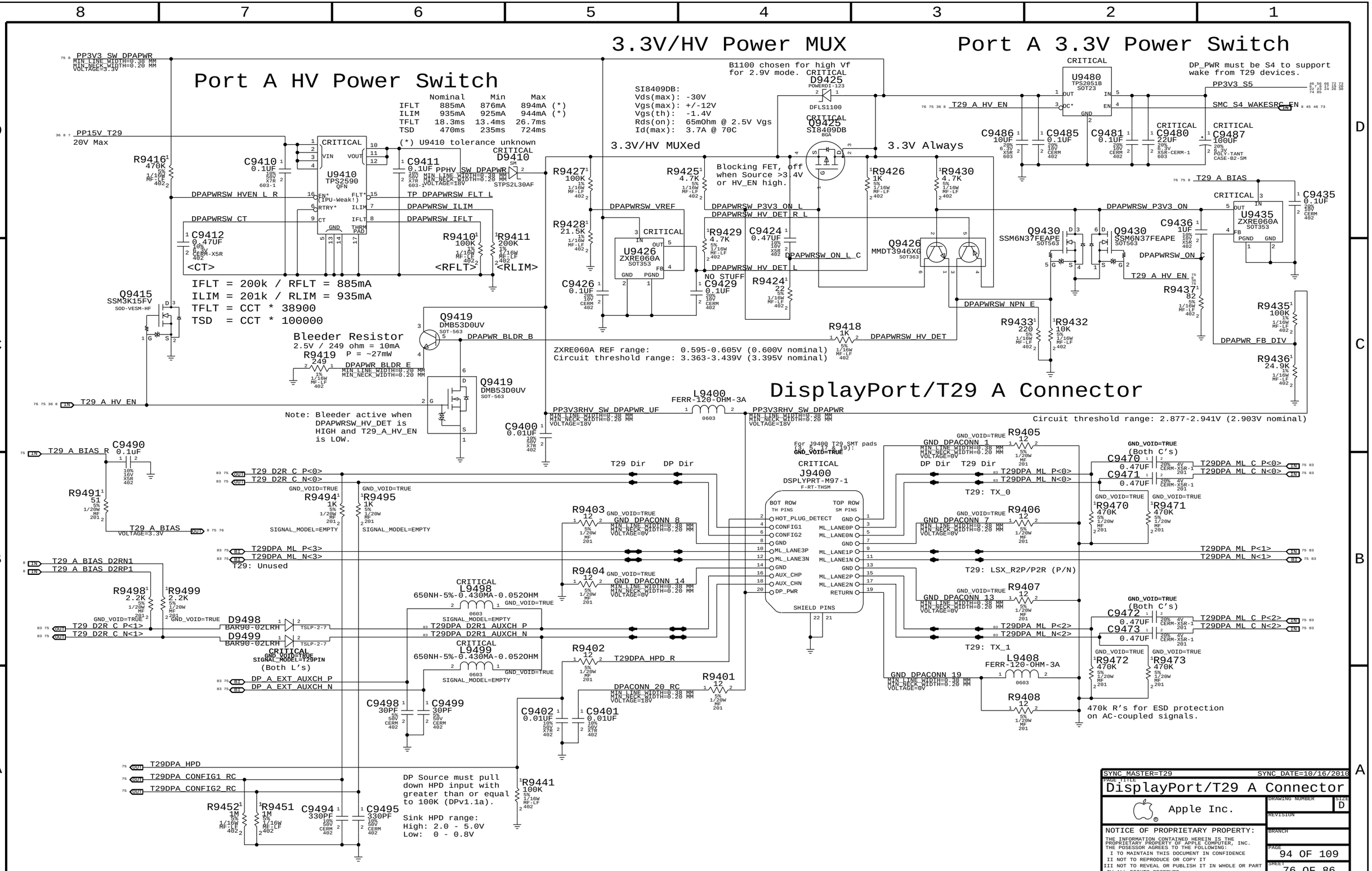

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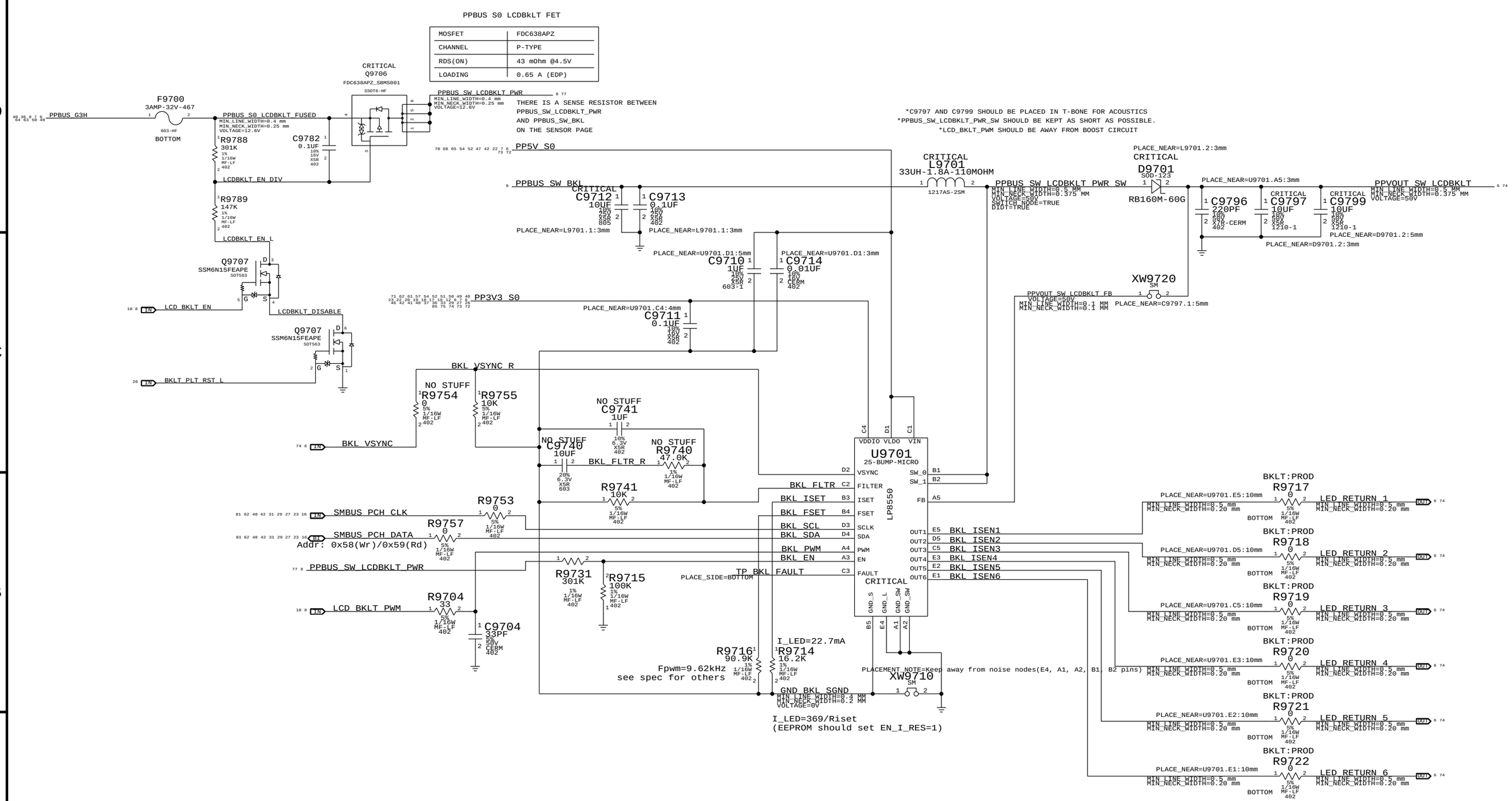

PART NUMBER	QTY	DESCRIPTION	REFERENCE DES	CRITICAL	BOM OPTION
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9717,R9718,R9719		BKLT:ENG
103S0198	3	RES,THIN FLIM,1/16W,10.2 OHM,0.1,0402,SM	R9720,R9721,R9722		BKLT:ENG

10.2 ohm resistors for current measurement on LED strings.

SYNC MASTER=VEMURI K90I SYNC DATE=06/25/2010

PAGE TITLE
LCD Backlight Driver

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CPU Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CPU_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CPU_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CPU_27P4S	*	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	=27P4_OHM_SE	7 MIL	7 MIL

NOTE: 7 mil gap is for VCCSense pair, which Intel says to route with 7 mil spacing without specifying a target impedance.

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	*	=STANDARD	?
CPU_8MIL	*	8 MIL	?
CPU_COMP	*	20 MIL	?
CPU_ITP	*	=2:1_SPACING	?
CPU_VCCSENSE	*	25 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CPU_AGTL	TOP,BOTTOM	=2x_DIELECTRIC	?

Most CPU signals with impedance requirements are 50-ohm single-ended.
Some signals require 27.4-ohm single-ended impedance.

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

PCI-Express

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

SOURCE: Huron River SFF DG (DG-438297_v1.0), Section 4.18 and Huron River Platform Power Delivery DG v1.0 Section 2.7

CPU Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_P<3:0>	9 17
DMI_S2N	PCIE_85D	PCIE	DMI_S2N_N<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_P<3:0>	9 17
DMI_N2S	PCIE_85D	PCIE	DMI_N2S_N<3:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_P<7:0>	9 17
FDI_DATA	PCIE_85D	PCIE	FDI_DATA_N<7:0>	9 17
	CPU_50S	CPU_AGTL	FDI_FSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_LSYNC<1..0>	9 17
	CPU_50S	CPU_AGTL	FDI_INT	9 17
CPU_PECI	CPU_50S	PCIE	CPU_PECI	10 19 45
PM_SYNC	CPU_50S	CPU_AGTL	PM_SYNC	10 17
PM_MEM_PWRGD	CPU_50S	CPU_AGTL	PM_MEM_PWRGD	10 17 30
	CPU_50S	CPU_ITP	XDP_DBRESET_L	10 23 26
	CPU_50S	CPU_ITP	XDP_CPU_PRDY_L	10 23
	CPU_50S	CPU_ITP	XDP_CPU_PREQ_L	10 23
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<0>	
	CPU_50S	CPU_AGTL	PM_EXT_TS_L<1>	
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<0>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<1>	10
CPU_SM_RCOMP	CPU_27P4S	CPU_COMP	CPU_SM_RCOMP<2>	10
	CPU_50S	CPU_ITP	CPU_CFG<11..0>	9 23
CPU_CATERR_L	CPU_50S	CPU_AGTL	CPU_CATERR_L	10
	CPU_50S	CPU_AGTL	CPU_VCCIO_SEL	12
CPU_PROCHOT_L	CPU_50S	CPU_AGTL	CPU_PROCHOT_L	10 46 68
CPU_PWRGD	CPU_50S	CPU_AGTL	CPU_PWRGD	10 19 23
PM_THRMTRIP_L	CPU_50S	CPU_8MIL	PM_THRMTRIP_L	10 19
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_P	10 16
DMI_CLK100M	CLK_PCIE_90D	CLK_PCIE	DMI_CLK100M_CPU_N	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_P	10 16
ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPCPU_CLK100M_N	10 16
[112] ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_P	16 23
[112] ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	ITPXDP_CLK100M_N	16 23
[112] ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_P	23
[112] ITPCPU_CLK100M	CLK_PCIE_90D	CLK_PCIE	XDP_CPU_CLK100M_N	23
[112]	CPU_27P4S	CPU_COMP	EDP_COMP	9
	CPU_27P4S	CPU_COMP	CPU_PEG_COMP	9
XDP_TDI	CPU_50S	CPU_ITP	XDP_CPU_TDI	10 23
XDP_TDO	CPU_50S	CPU_ITP	XDP_CPU_TDO	10 23
XDP_TMS	CPU_50S	CPU_ITP	XDP_CPU_TMS	10 23
XDP_TCK	CPU_50S	CPU_ITP	XDP_CPU_TCK	10 23
XDP_TRST_L	CPU_50S	CPU_ITP	XDP_CPU_TRST_L	10 23
XDP_BPM_L	CPU_50S	CPU_ITP	XDP_BPM_L<3..0>	10 23
XDP_BPM_R_L	CPU_50S	CPU_ITP	CPU_CFG<15..12>	9 23
(FSB_CPURST_L)	CPU_50S	CPU_ITP	XDP_CPURST_L	23
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCSENSE_N	12 68
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_P	12 70
CPU_VCCSENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCCIOSENSE_N	12 70
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_P	12 68
CPU_VCCAXG_SENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_SENSE_N	12 68
[112] CPU_VAISENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_P	12
[112] CPU_VAISENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VDDQ_SENSE_N	12
[112] CPU_VAISENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_P	9
[112] CPU_VAISENSE	CPU_27P4S	CPU_VCCSENSE	CPU_AXG_VALSENSE_N	9
[112] CPU_VAISENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_P	9
[112] CPU_VAISENSE	CPU_27P4S	CPU_VCCSENSE	CPU_VCC_VALSENSE_N	9
[112] CPU_SVIDALERT_L	CPU_50S	CPU_COMP	CPU_VIDALERT_L	12 68
[112] CPU_SVIDSCLK	CPU_50S	CPU_COMP	CPU_VIDSCLK	12 68
[112] CPU_SVIDSOUT	CPU_50S	CPU_COMP	CPU_VIDSOUT	12 68
	PCIE_85D	PCIE	PEG_R2D_P<15..0>	
	PCIE_85D	PCIE	PEG_R2D_N<15..0>	
PEG_R2D	PCIE_85D	PCIE	PEG_R2D_C_P<15..0>	8
	PCIE_85D	PCIE	PEG_R2D_C_N<15..0>	8
PEG_D2R	PCIE_85D	PCIE	PEG_D2R_P<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_N<15..0>	8
	PCIE_85D	PCIE	PEG_D2R_C_P<15..0>	
	PCIE_85D	PCIE	PEG_D2R_C_N<15..0>	

CPU_VCCSA_VID<0>
CPU_VCCSA_VID<1>

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Memory Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_37S	*	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=37_OHM_SE	=STANDARD	=STANDARD
MEM_40S	*	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=40_OHM_SE	=STANDARD	=STANDARD
MEM_72D	*	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF	=72_OHM_DIFF
MEM_50S	TOP,BOTTOM	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	TOP,BOTTOM	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL10	N	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL10	N	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
MEM_50S	ISL3,ISL4,ISL9	Y	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
MEM_85D	ISL3,ISL4,ISL9	Y	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
MEM_CLK2MEM	*	=4:1_SPACING	?
MEM_CTRL2CTRL	*	=3:1_SPACING	?
MEM_CTRL2MEM	*	=2.5:1_SPACING	?
MEM_CMD2CMD	*	=1.5:1_SPACING	?
MEM_CMD2MEM	*	=3:1_SPACING	?
MEM_DATA2DATA	*	=1.5:1_SPACING	?
MEM_DATA2MEM	*	=3:1_SPACING	?
MEM_DQS2MEM	*	=3:1_SPACING	?
MEM_2OTHER	*	25 MILS	?

Memory Bus Spacing Group Assignments

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	MEM_CLK	*	MEM_CLK2MEM
MEM_CLK	MEM_CTRL	*	MEM_CLK2MEM
MEM_CLK	MEM_CMD	*	MEM_CLK2MEM
MEM_CLK	MEM_DATA	*	MEM_CLK2MEM
MEM_CLK	MEM_DQS	*	MEM_CLK2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CMD	MEM_CLK	*	MEM_CMD2MEM
MEM_CMD	MEM_CTRL	*	MEM_CMD2MEM
MEM_CMD	MEM_CMD	*	MEM_CMD2CMD
MEM_CMD	MEM_DATA	*	MEM_CMD2MEM
MEM_CMD	MEM_DQS	*	MEM_CMD2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CTRL	MEM_CLK	*	MEM_CTRL2MEM
MEM_CTRL	MEM_CTRL	*	MEM_CTRL2CTRL
MEM_CTRL	MEM_CMD	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DATA	*	MEM_CTRL2MEM
MEM_CTRL	MEM_DQS	*	MEM_CTRL2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DATA	MEM_CLK	*	MEM_DATA2MEM
MEM_DATA	MEM_CTRL	*	MEM_DATA2MEM
MEM_DATA	MEM_CMD	*	MEM_DATA2MEM
MEM_DATA	MEM_DATA	*	MEM_DATA2DATA
MEM_DATA	MEM_DQS	*	MEM_DATA2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_DQS	MEM_CLK	*	MEM_DQS2MEM
MEM_DQS	MEM_CTRL	*	MEM_DQS2MEM
MEM_DQS	MEM_CMD	*	MEM_DQS2MEM
MEM_DQS	MEM_DATA	*	MEM_DQS2MEM
MEM_DQS	MEM_DQS	*	MEM_DQS2MEM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	*	*	MEM_2OTHER
MEM_CTRL	*	*	MEM_2OTHER
MEM_CMD	*	*	MEM_2OTHER
MEM_DATA	*	*	MEM_2OTHER
MEM_DQS	*	*	MEM_2OTHER

Need to support MEM_*-style wildcards!

DDR3: Sandybridge SFF 2C when routed on Type-3 (Through hole) should follow rPGA guidelines per Huron River SFF DG rev1.0 (#438297).
DQS intra-pair matching should be within 0.127mm, no inter-pair matching requirement.
DQ to DQS matching per byte lane should be within 0.127mm.
DQS to clock matching should be within [CLK-63.5mm] and [CLK+38.1mm].
CLK intra-pair matching should be within 0.127mm, inter-pair matching should be within 0.0508mm.
CONTROL signals should be matched within [CLK-2.54mm] to [CLK+0.0mm] of CLK pairs.
A/BA/CMD signals should be matched within [CLK-12.7mm] to [CLK+12.7mm] of CLK pairs A/BA/CMD signals to each other should match within 5.08mm.
DQ/DQS/A/BA/cmd signal spacing is 4x dielectric, CLK is 5x dielectric.
Maximum length of any signal from die pad to SODIMM pad is 119.83mm, from procesor ball to SODIMM pad is 88.9mm.
SOURCE: Huron River Platform DG, Rev 1.01 (#436735), Section 2.5

Memory Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_P<5..0>	11 27
MEM_A_CLK	MEM_72D	MEM_CLK	MEM_A_CLK_N<5..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CKE<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_CS_L<3..0>	11 27
MEM_A_CNTL	MEM_37S	MEM_CTRL	MEM_A_ODT<3..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_A<15..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_BA<2..0>	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_RAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_CAS_L	11 27
MEM_A_CMD	MEM_40S	MEM_CMD	MEM_A_WE_L	11 27
MEM_A_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_A_DQ<7..0>	11 28
MEM_A_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_A_DQ<15..8>	11 28
MEM_A_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_A_DQ<23..16>	11 28
MEM_A_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_A_DQ<31..24>	11 28
MEM_A_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_A_DQ<39..32>	11 27 28
MEM_A_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_A_DQ<47..40>	11 28
MEM_A_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_A_DQ<55..48>	11 28
MEM_A_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_A_DQ<63..56>	11 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_P<0>	11 27 28
MEM_A_DQS0	MEM_85D	MEM_DQS	MEM_A_DQS_N<0>	11 27 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_P<1>	11 28
MEM_A_DQS1	MEM_85D	MEM_DQS	MEM_A_DQS_N<1>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_P<2>	11 28
MEM_A_DQS2	MEM_85D	MEM_DQS	MEM_A_DQS_N<2>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_P<3>	11 28
MEM_A_DQS3	MEM_85D	MEM_DQS	MEM_A_DQS_N<3>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_P<4>	11 28
MEM_A_DQS4	MEM_85D	MEM_DQS	MEM_A_DQS_N<4>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_P<5>	11 28
MEM_A_DQS5	MEM_85D	MEM_DQS	MEM_A_DQS_N<5>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_P<6>	11 28
MEM_A_DQS6	MEM_85D	MEM_DQS	MEM_A_DQS_N<6>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_P<7>	11 28
MEM_A_DQS7	MEM_85D	MEM_DQS	MEM_A_DQS_N<7>	11 28
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_P<5..0>	11 29
MEM_B_CLK	MEM_72D	MEM_CLK	MEM_B_CLK_N<5..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CKE<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_CS_L<3..0>	11 29
MEM_B_CNTL	MEM_37S	MEM_CTRL	MEM_B_ODT<3..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_A<15..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_BA<2..0>	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_RAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_CAS_L	11 29
MEM_B_CMD	MEM_40S	MEM_CMD	MEM_B_WE_L	11 29
MEM_B_DQ_BYTE0	MEM_50S	MEM_DATA	MEM_B_DQ<7..0>	11 28
MEM_B_DQ_BYTE1	MEM_50S	MEM_DATA	MEM_B_DQ<15..8>	11 28
MEM_B_DQ_BYTE2	MEM_50S	MEM_DATA	MEM_B_DQ<23..16>	11 28
MEM_B_DQ_BYTE3	MEM_50S	MEM_DATA	MEM_B_DQ<31..24>	11 28
MEM_B_DQ_BYTE4	MEM_50S	MEM_DATA	MEM_B_DQ<39..32>	11 28 29
MEM_B_DQ_BYTE5	MEM_50S	MEM_DATA	MEM_B_DQ<47..40>	11 28
MEM_B_DQ_BYTE6	MEM_50S	MEM_DATA	MEM_B_DQ<55..48>	11 28
MEM_B_DQ_BYTE7	MEM_50S	MEM_DATA	MEM_B_DQ<63..56>	11 28
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_P<0>	11 28 29
MEM_B_DQS0	MEM_85D	MEM_DQS	MEM_B_DQS_N<0>	11 28 29
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_P<1>	11 28
MEM_B_DQS1	MEM_85D	MEM_DQS	MEM_B_DQS_N<1>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_P<2>	11 28
MEM_B_DQS2	MEM_85D	MEM_DQS	MEM_B_DQS_N<2>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_P<3>	11 28
MEM_B_DQS3	MEM_85D	MEM_DQS	MEM_B_DQS_N<3>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_P<4>	11 28
MEM_B_DQS4	MEM_85D	MEM_DQS	MEM_B_DQS_N<4>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_P<5>	11 28
MEM_B_DQS5	MEM_85D	MEM_DQS	MEM_B_DQS_N<5>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_P<6>	11 28
MEM_B_DQS6	MEM_85D	MEM_DQS	MEM_B_DQS_N<6>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_P<7>	11 28
MEM_B_DQS7	MEM_85D	MEM_DQS	MEM_B_DQS_N<7>	11 28

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Digital Video Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
LVDS_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?
LVDS	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?
LVDS	TOP,BOTTOM	=4x_DIELECTRIC	?

LVDS intra-pair matching should be 5 mils. Pairs should be within 100 mils of clock length.
DisplayPort/TMDS intra-pair matching should be 5 ps. Inter-pair matching should be within 150 ps.
DIsplayPort AUX CH intra-pair matching should be 5 ps. No relationship to other signals.
Max length of LVDS/DisplayPort/TMDS traces: 12 inches.
SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Sections 2.5.3 & 2.5.4.

SATA Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SATA_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	*	=4x_DIELECTRIC	?
SATA_ICOMP	*	8 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SATA	TOP,BOTTOM	=3x_DIELECTRIC	?

SOURCE: MCP79 Interface DG (DG-03328-001_v0D), Section 2.7.1.

USB 2.0 Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCH_USB_RBIAS	*	=STANDARD	8 MIL	8 MIL	=STANDARD	=STANDARD	=STANDARD
USB_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	*	=2x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
USB	TOP,BOTTOM	=4x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.8

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_P<3..0>	8
DP_ML	DP_85D	DISPLAYPORT	DP_IG_ML_N<3..0>	8
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 17 75 81
DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 17 75 81
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_P	18 74
LVDS_IG_A_CLK	LVDS_90D	LVDS	LVDS_IG_A_CLK_N	18 74
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_P<2..0>	6 18 74
LVDS_IG_A_DATA	LVDS_90D	LVDS	LVDS_IG_A_DATA_N<2..0>	6 18 74
	LVDS_90D	LVDS	NC_LVDS_IG_A_DATAP<3>	8 18
	LVDS_90D	LVDS	NC_LVDS_IG_A_DATAN<3>	8 18
	LVDS_90D	LVDS	LVDS_IG_B_DATA_P<3..0>	8
	LVDS_90D	LVDS	LVDS_IG_B_DATA_N<3..0>	8
	LVDS_90D	LVDS	TP_LVDS_IG_B_CLKP	6 8 18
	LVDS_90D	LVDS	TP_LVDS_IG_B_CLKN	6 8 18
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_P	16 42
SATA_HDD_R2D	SATA_90D	SATA	SATA_HDD_R2D_C_N	16 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_P	6 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_N	6 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_P	16 42
SATA_HDD_D2R	SATA_90D	SATA	SATA_HDD_D2R_N	16 42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_C_P	6 42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_C_N	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_P	16 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_C_N	16 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_P	6 42
SATA_ODD_R2D	SATA_90D	SATA	SATA_ODD_R2D_N	6 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_P	16 42
SATA_ODD_D2R	SATA_90D	SATA	SATA_ODD_D2R_N	16 42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_RC_P	42
SATA_HDD_R2D_CONN	SATA_90D	SATA	SATA_HDD_R2D_RC_N	42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_RC_P	42
SATA_HDD_D2R_CONN	SATA_90D	SATA	SATA_HDD_D2R_RC_N	42
PCH_SATA_ICOMP		SATA_ICOMP	PCH_SATAICOMP	16
USB_HUB1_UP	USB_85D	USB	USB_HUB1_UP_P	18 24
	USB_85D	USB	USB_HUB1_UP_N	18 24
USB_HUB2_UP	USB_85D	USB	USB_HUB2_UP_P	18 24
	USB_85D	USB	USB_HUB2_UP_N	18 24
USB_EXTA	USB_85D	USB	USB_EXTA_P	24 43
USB_EXTA	USB_85D	USB	USB_EXTA_N	24 43
USB_EXTB	USB_85D	USB	USB_EXTB_P	24 43
	USB_85D	USB	USB_EXTB_N	24 43
USB_EXTC	USB_85D	USB	USB_EXTC_P	8 24
	USB_85D	USB	USB_EXTC_N	8 24
USB_EXTD	USB_85D	USB	USB_T29A_P	8 24
	USB_85D	USB	USB_T29A_N	8 24
	USB_85D	USB	T29_A_RSVD_P	8 75
	USB_85D	USB	T29_A_RSVD_N	8 75
USB_CAMERA	USB_85D	USB	USB_CAMERA_P	18 32
	USB_85D	USB	USB_CAMERA_N	18 32
USB_CAMERA	USB_85D	USB	USB_CAMERA_CONN_P	6 32
	USB_85D	USB	USB_CAMERA_CONN_N	6 32
USB_BT	USB_85D	USB	USB_BT_P	6 24 32
USB_BT	USB_85D	USB	USB_BT_N	6 24 32
USB_TPAD	USB_85D	USB	USB_TPAD_P	24 53
	USB_85D	USB	USB_TPAD_N	24 53
USB_IR	USB_85D	USB	USB_IR_P	24 44
	USB_85D	USB	USB_IR_N	24 44
USB_SDCARD	USB_85D	USB	USB_SDCARD_P	
	USB_85D	USB	USB_SDCARD_N	
USB_BRCRYPT	USB_85D	USB	USB_BRCRYPT_P	
	USB_85D	USB	USB_BRCRYPT_N	
PCH_USB_RBIAS	PCH_USB_RBIAS		PCH_USB_RBIAS	18
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_P	16 25
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_PCH_N	16 25
	CLK_PCIE_90D	CLK_PCIE	NC_FSB_CLK133M_PCH_P	8
	CLK_PCIE_90D	CLK_PCIE	NC_FSB_CLK133M_PCH_N	8
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_P	16 25
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK96M_DOT_N	16 25
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_P	16 25
PCH_DIFFCLK_UNUSED	CLK_PCIE_90D	CLK_PCIE	PCH_CLK100M_SATA_N	16 25
	CPU_50S	CLK_PCIE	PCH_CLK14P3M_REFCLK	16 25
LPC_CLK33M	CPU_50S	CLK_PCIE	PCH_CLK33M_PCIIN	16 26
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_P	
GFX_CLK_DPLLSS	CLK_PCIE_90D	CLK_PCIE	GFX_CLK120M_DPLLSS_N	

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LPC Bus Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD
CLK_LPC_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
LPC	*	6 MIL	?
CLK_LPC	*	8 MIL	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SMBus Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SMB_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SMB	*	=2x_DIELECTRIC	?

HD Audio Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
HDA_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
HDA	*	=2x_DIELECTRIC	?

SOURCE: Calpella Platform Design Guide for Ibex Peak M (DG-398905-398905_v1.5), Section 3.15

SIO Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	8 MIL	?

SPI Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SPI	*	8 MIL	?

DisplayPort Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DP_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	*	=3x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DISPLAYPORT	TOP,BOTTOM	=4x_DIELECTRIC	?

PCI-Express Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
PCIE_85D	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
CLK_PCIE_90D	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	*	=3X_DIELECTRIC	?
CLK_PCIE	*	20 MIL	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
PCIE	TOP,BOTTOM	=4X_DIELECTRIC	?

System Clock Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
CLK_SLOW_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD
CLK_25M_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
CLK_SLOW	*	=2x_DIELECTRIC	?
CLK_25M	*	=5x_DIELECTRIC	?

NOTE: 25MHz system clocks very sensitive to noise.

PCH Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
LPC_AD	LPC_50S	LPC	LPC_AD<3..0>	6 16 45 47
LPC_FRAME_L	LPC_50S	LPC	LPC_FRAME_L	6 16 45 47
LPC_RESET_L	LPC_50S	LPC	LPCPLUS_RESET_L	6 26 47
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC_R	18 26
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_SMC	26 45
LPC_CLK33M	CLK_LPC_50S	CLK_LPC	LPC_CLK33M_LPCPLUS	6 26 47
SMBUS_PCH_CLK	SMB_50S	SMB	SMBUS_PCH_CLK	16 23 27 29 31 42 48 62 77
SMBUS_PCH_DATA	SMB_50S	SMB	SMBUS_PCH_DATA	16 23 27 29 31 42 48 62 77
SMBUS_PCH_0_CLK	SMB_50S	SMB	SML_PCH_0_CLK	16 48
SMBUS_PCH_0_DATA	SMB_50S	SMB	SML_PCH_0_DATA	16 48
SMBUS_PCH_1_CLK	SMB_50S	SMB	SML_PCH_1_CLK	16 48
SMBUS_PCH_1_DATA	SMB_50S	SMB	SML_PCH_1_DATA	16 48
HDA_BIT_CLK	HDA_50S	HDA	HDA_BIT_CLK	16 57
	HDA_50S	HDA	HDA_BIT_CLK_R	16
HDA_SYNC	HDA_50S	HDA	HDA_SYNC	16 57
	HDA_50S	HDA	HDA_SYNC_R	16
HDA_RST_L	HDA_50S	HDA	HDA_RST_R_L	16
	HDA_50S	HDA	HDA_RST_L	16 57
HDA_SDIN0	HDA_50S	HDA	HDA_SDIN0	16 57
	HDA_50S	HDA	AUD_SDI_R	67
HDA_SDOUT	HDA_50S	HDA	HDA_SDOUT	16 57
	HDA_50S	HDA	HDA_SDOUT_R	16
PM_SUS_CLK	CLK_SLOW_55S	CLK_SLOW	PM_CLK32K_SUSCLK	
SPI_CLK	SPI_55S	SPI	SPI_CLK_R	16 47
	SPI_55S	SPI	SPI_CLK	47
SPI_MOSI	SPI_55S	SPI	SPI_MOSI_R	16 47
	SPI_55S	SPI	SPI_MOSI	47
SPI_MISO	SPI_55S	SPI	SPI_MISO	16 47
SPI_CS0	SPI_55S	SPI	SPI_CS0_R_L	16 47
	SPI_55S	SPI	SPI_CS0_L	47
	PCIE_85D	PCIE	PCIE_ENET_R2D_P	37
	PCIE_85D	PCIE	PCIE_ENET_R2D_N	37
PCIE_ENET_R2D	PCIE_85D	PCIE	PCIE_ENET_R2D_C_P	16 37
	PCIE_85D	PCIE	PCIE_ENET_R2D_C_N	16 37
PCIE_ENET_D2R	PCIE_85D	PCIE	PCIE_ENET_D2R_P	16 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_N	16 37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_P	37
	PCIE_85D	PCIE	PCIE_ENET_D2R_C_N	37
	PCIE_85D	PCIE	PCIE_AP_R2D_P	6 32
	PCIE_85D	PCIE	PCIE_AP_R2D_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_C_P	16 32
	PCIE_85D	PCIE	PCIE_AP_R2D_C_N	16 32
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_P	16 32
	PCIE_85D	PCIE	PCIE_AP_D2R_N	16 32
	PCIE_85D	PCIE	PCIE_FW_R2D_P	39
	PCIE_85D	PCIE	PCIE_FW_R2D_N	39
PCIE_FW_R2D	PCIE_85D	PCIE	PCIE_FW_R2D_C_P	16 39
	PCIE_85D	PCIE	PCIE_FW_R2D_C_N	16 39
PCIE_FW_D2R	PCIE_85D	PCIE	PCIE_FW_D2R_P	16 39
	PCIE_85D	PCIE	PCIE_FW_D2R_N	16 39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_P	39
	PCIE_85D	PCIE	PCIE_FW_D2R_C_N	39
PCIE_AP_D2R	PCIE_85D	PCIE	PCIE_AP_D2R_PI_P	6 32
	PCIE_85D	PCIE	PCIE_AP_D2R_PI_N	6 32
PCIE_AP_R2D	PCIE_85D	PCIE	PCIE_AP_R2D_PI_P	32
	PCIE_85D	PCIE	PCIE_AP_R2D_PI_N	32
	CLK_PCIE_90D	CLK_PCIE	NC_PEG_CLK100MP	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PEG_CLK100MN	8 16
PCIE_CLK100M_ENET	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_P	16 37
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_ENET_N	16 37
MCP_PE1_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_P	16 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_N	16 32
MCP_PE2_REFCLK	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_P	16 39
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_FW_N	16 39
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDP	8 16
	CLK_PCIE_90D	CLK_PCIE	NC_PCIE_CLK100M_EXCARDN	8 16
B35	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<1>	6
B36	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<2>	6
B37	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<5>	6
B38	CPU_27P4S	CPU_COMP	TP_PCH_VSS_NCTF<7>	
B39	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 81
B40	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<9>	6 81
B41	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<11>	6
B42	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<12>	6
B43	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<15>	6
B44	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<17>	6
B45	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<19>	6
B46	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<21>	6
B47	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<22>	
B48	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<25>	6
B49	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<27>	6
B50	CPU_27P4S	CPU_COMP	PCH_VSS_NCTF<29>	6

Chipset Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T252	DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_P<3..0>	8 75
T253	DP_EXTA_ML	DP_85D	DISPLAYPORT	DP_EXTA_ML_C_N<3..0>	8 75
T253		DP_85D	DISPLAYPORT	DP_EXTA_ML_P<3..0>	75
T255		DP_85D	DISPLAYPORT	DP_EXTA_ML_N<3..0>	75
T256	DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_P	8 17 75 80
T257	DP_EXTA_AUXCH	DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_C_N	8 17 75 80
T267		DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_P	75
T258		DP_85D	DISPLAYPORT	DP_EXTA_AUXCH_N	75
T267	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_P<3..0>	
T268	DP_INT_ML	DP_85D	DISPLAYPORT	DP_INT_ML_C_N<3..0>	
T269	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_P	
T270	DP_INT_AUXCH	DP_85D	DISPLAYPORT	DP_INT_AUXCH_C_N	
T271	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_P<3..0>	8 34
T273	PCIE_T29_R2D	PCIE_85D	PCIE	PCIE_T29_R2D_C_N<3..0>	8 34
T272		PCIE_85D	PCIE	PCIE_T29_R2D_P<3..0>	34
T274		PCIE_85D	PCIE	PCIE_T29_R2D_N<3..0>	34
T276	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_P<3..0>	8 34
T275	PCIE_T29_D2R	PCIE_85D	PCIE	PCIE_T29_D2R_N<3..0>	8 34
T277		PCIE_85D	PCIE	PCIE_T29_D2R_C_P<3..0>	34
T278		PCIE_85D	PCIE	PCIE_T29_D2R_C_N<3..0>	34
T279	PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_P	16 34
T280	PCIE_CLK100M_T29	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_T29_N	16 34

Clock Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
T281	SYSCLK_CLK32K_RTC	CLK_SLOW_55S	CLK_SLOW	SYSCLK_CLK32K_RTC	16 26
T282	SYSCLK_CLK25M_SB	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB	16 26
T283		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_SB_R	16
T284		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET	26 37
T285		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_ENET_R
T286	SYSCLK_CLK25M_T29	CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29	26 34
T287		CLK_25M_55S	CLK_25M	SYSCLK_CLK25M_T29_R	34

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CAESAR IV (Ethernet) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_50S	*	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=50_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_3X	*	=3:1_SPACING	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_CR_DATA	*	8MIL	?

CAESAR IV (Ethernet PHY) Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
ENET_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENET_MDI	*	0.6 MM	?

SOURCE: Broadcom 5764-DS04-RDS Page 38

FireWire Interface Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
FW_110D	*	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF	=110_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
FW_TP	*	=3:1_SPACING	?

Ethernet Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
		ENET_50S	ENET_3X	BCM5764_CLK25M_XTALI	
		ENET_50S	ENET_3X	BCM5764_CLK25M_XTALO	
		ENET_50S	ENET_3X	ENET_RESET_L	33 37
	ENET_MDI	ENET_100D	ENET_MDI	ENET_MDI_P<3..0>	37 38
		ENET_100D	ENET_MDI	ENET_MDI_N<3..0>	37 38
I162	CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_DATA<7..0>	33 37
I167	CR_DATA	ENET_50S	ENET_CR_DATA	ENET_CR_CMD	33 37
I163	CR_CLK	ENET_50S	ENET_CR_DATA	ENET_CR_CLK	33 37
I160	CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_DATA<7..0>	33
I172	CR_DATA	ENET_50S	ENET_CR_DATA	SDCONN_CMD	33
I171	CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK	33
I170	CR_CLK	ENET_50S	ENET_CR_DATA	SDCONN_CLK_L	33

FireWire Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
I150	FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAP	6 39 41
I150	FW_P0_TPA	FW_110D	FW_TP	NC_FW0_TPAN	39 41
I160	FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBP	6 39 41
I160	FW_P0_TPB	FW_110D	FW_TP	NC_FW0_TPBN	6 39 41
I162	FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_P	39 41
I162	FW_P1_TPA	FW_110D	FW_TP	FW_PORT1_TPA_N	39 41
I163	FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_P	39 41
I163	FW_P1_TPB	FW_110D	FW_TP	FW_PORT1_TPB_N	39 41

Port 2 Not Used

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DisplayPort Signal Constraints

NOTE: DisplayPort Physical/Spacing Constraints provided by Chipset or GPU page.

T29 I2C Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_I2C_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_I2C	*	=2x_DIELECTRIC	?

T29 SPI Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29_SPI_55S	*	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=STANDARD	=STANDARD

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29_SPI	*	=2x_DIELECTRIC	?

T29/DP Connector Signal Constraints

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
T29DP_80D	*	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF	=80_OHM_DIFF
T29DP_100D	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	*	=5x_DIELECTRIC	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
T29DP	TOP,BOTTOM	=7x_DIELECTRIC	?

SOURCE: Bill Cornelius's T29 Routing Notes

T29/DP Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
161	T29_R2D0	T29DP_80D	T29DP	T29_R2D_P<0>	75
162	T29_R2D0	T29DP_80D	T29DP	T29_R2D_N<0>	75
163	T29_R2D1	T29DP_80D	T29DP	T29_R2D_P<1>	75
164	T29_R2D1	T29DP_80D	T29DP	T29_R2D_N<1>	75
165		T29DP_80D	T29DP	T29_R2D_C_F_P<1..0>	75
166		T29DP_80D	T29DP	T29_R2D_C_F_N<1..0>	75
167	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_P<0>	75 76
168	T29_D2R0	T29DP_100D	T29DP	T29_D2R_C_N<0>	75 76
169	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_P<1>	75 76
170	T29_D2R1	T29DP_100D	T29DP	T29_D2R_C_N<1>	75 76
171		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_P	76
172		T29DP_100D	T29DP	T29DPA_D2R1_AUXCH_N	76
173		T29DP_80D	T29DP	DP_SDRVA_ML_C_P<3..0>	75
174		T29DP_80D	T29DP	DP_SDRVA_ML_C_N<3..0>	75
175		T29DP_80D	T29DP	DP_SDRVA_ML_R_P<3..0>	75
176		T29DP_80D	T29DP	DP_SDRVA_ML_R_N<3..0>	75
177	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_P<2..0:2>	75 83
178	DP_SDRVA_ML_EVEN	T29DP_80D	T29DP	DP_SDRVA_ML_N<2..0:2>	75 83
179	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_P<3..1:2>	75
180	DP_SDRVA_ML_ODD	T29DP_80D	T29DP	DP_SDRVA_ML_N<3..1:2>	75
181	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_P	75
182	DP_SDRVA_AUXCH	T29DP_80D	T29DP	DP_SDRVA_AUXCH_N	75
183		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_P	75
184		T29DP_80D	T29DP	DP_SDRVA_AUXCH_C_N	75
185		T29DP_80D	T29DP	T29DPA_ML_P<3..0>	75 76
186		T29DP_80D	T29DP	T29DPA_ML_N<3..0>	75 76
187		T29DP_80D	T29DP	T29DPA_ML_C_P<3..0>	75 76
188		T29DP_80D	T29DP	T29DPA_ML_C_N<3..0>	75 76
189		T29DP_80D	T29DP	DP_A_EXT_AUXCH_P	75 76
190		T29DP_80D	T29DP	DP_A_EXT_AUXCH_N	75 76
191	T29_R2D2	T29DP_80D	T29DP	T29_R2D_P<2>	
192	T29_R2D2	T29DP_80D	T29DP	T29_R2D_N<2>	
193	T29_R2D3	T29DP_80D	T29DP	T29_R2D_P<3>	
194	T29_R2D3	T29DP_80D	T29DP	T29_R2D_N<3>	
195		T29DP_80D	T29DP	T29_R2D_C_F_P<3..2>	
196		T29DP_80D	T29DP	T29_R2D_C_F_N<3..2>	
197	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_P<2>	
198	T29_D2R2	T29DP_100D	T29DP	T29_D2R_C_N<2>	
199	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_P<3>	
200	T29_D2R3	T29DP_100D	T29DP	T29_D2R_C_N<3>	
201		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_P	
202		T29DP_100D	T29DP	T29DPB_D2R3_AUXCH_N	
203		T29DP_80D	T29DP	DP_SDRVB_ML_C_P<3..0>	
204		T29DP_80D	T29DP	DP_SDRVB_ML_C_N<3..0>	
205		T29DP_80D	T29DP	DP_SDRVB_ML_R_P<3..0>	
206		T29DP_80D	T29DP	DP_SDRVB_ML_R_N<3..0>	
207	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_P<2..0:2>	83
208	DP_SDRVB_ML_EVEN	T29DP_80D	T29DP	DP_SDRVB_ML_N<2..0:2>	83
209	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_P<3..1:2>	
210	DP_SDRVB_ML_ODD	T29DP_80D	T29DP	DP_SDRVB_ML_N<3..1:2>	
211	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_P	
212	DP_SDRVB_AUXCH	T29DP_80D	T29DP	DP_SDRVB_AUXCH_N	
213		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_P	
214		T29DP_80D	T29DP	DP_SDRVB_AUXCH_C_N	
215		T29DP_80D	T29DP	T29DPB_ML_P<3..0>	
216		T29DP_80D	T29DP	T29DPB_ML_N<3..0>	
217		T29DP_80D	T29DP	T29DPB_ML_C_P<3..0>	
218		T29DP_80D	T29DP	T29DPB_ML_C_N<3..0>	
219		T29DP_80D	T29DP	DP_B_EXT_AUXCH_P	
220		T29DP_80D	T29DP	DP_B_EXT_AUXCH_N	

Only used on dual-port hosts.

T29 IC Net Properties

	ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
162		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_P<3..0>	8 34
163		DP_85D	DISPLAYPORT	DP_T29SNK0_ML_C_N<3..0>	8 34
163	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_P<3..0>	34
164	DP_T29SNK0_ML	DP_85D	DISPLAYPORT	DP_T29SNK0_ML_N<3..0>	34
165		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_P	8 17 34
166		DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_C_N	8 17 34
167	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_P	34
168	DP_T29SNK0_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK0_AUXCH_N	34
169		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_P<3..0>	8 34
170		DP_85D	DISPLAYPORT	DP_T29SNK1_ML_C_N<3..0>	8 34
171	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_P<3..0>	34
172	DP_T29SNK1_ML	DP_85D	DISPLAYPORT	DP_T29SNK1_ML_N<3..0>	34
174		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_P	8 17 34
173		DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_C_N	8 17 34
175	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_P	34
176	DP_T29SNK1_AUXCH	DP_85D	DISPLAYPORT	DP_T29SNK1_AUXCH_N	34
177		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_P<3..0>	
178		DP_85D	DISPLAYPORT	DP_T29SRC_ML_C_N<3..0>	
179		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_P	
180		DP_85D	DISPLAYPORT	DP_T29SRC_AUXCH_C_N	
181		T29_I2C_55S	T29_I2C	I2C_T29_SCL	34 48 75
182		T29_I2C_55S	T29_I2C	I2C_T29_SDA	34 48 75
183	T29_SPI_CLK	T29_SPI_55S	T29_SPI	T29_SPI_CLK	34
184	T29_SPI_MOSI	T29_SPI_55S	T29_SPI	T29_SPI_MOSI	34
185	T29_SPI_MISO	T29_SPI_55S	T29_SPI	T29_SPI_MISO	34
186	T29_SPI_CS_L	T29_SPI_55S	T29_SPI	T29_SPI_CS_L	34
187		T29DP_80D	T29DP	T29_R2D_C_P<3..0>	8 34 75
188		T29DP_80D	T29DP	T29_R2D_C_N<3..0>	8 34 75
189		T29DP_100D	T29DP	T29_D2R_P<3..0>	8 34 75
190		T29DP_100D	T29DP	T29_D2R_N<3..0>	8 34 75

Only used on hosts supporting T29 video-in

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1T01_DIFFPAIR	*	=STANDARD	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

SMC SMBus Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
SMBUS_SMC_A_S3_SCL	SMB_50S	SMB	SMBUS_SMC_A_S3_SCL	6 32 45 48 54 55
SMBUS_SMC_A_S3_SDA	SMB_50S	SMB	SMBUS_SMC_A_S3_SDA	6 32 45 48 54 55
SMBUS_SMC_B_S0_SCL	SMB_50S	SMB	SMBUS_SMC_B_S0_SCL	45 48 51
SMBUS_SMC_B_S0_SDA	SMB_50S	SMB	SMBUS_SMC_B_S0_SDA	45 48 51
SMBUS_SMC_0_S0_SCL	SMB_50S	SMB	SMBUS_SMC_0_S0_SCL	6 32 45 48 51
SMBUS_SMC_0_S0_SDA	SMB_50S	SMB	SMBUS_SMC_0_S0_SDA	6 32 45 48 51
SMBUS_SMC_BSA_SCL	SMB_50S	SMB	SMBUS_SMC_BSA_SCL	6 45 48 63 64
SMBUS_SMC_BSA_SDA	SMB_50S	SMB	SMBUS_SMC_BSA_SDA	6 45 48 63 64
SMBUS_SMC_MGMT_SCL	SMB_50S	SMB	SMBUS_SMC_MGMT_SCL	45 48
SMBUS_SMC_MGMT_SDA	SMB_50S	SMB	SMBUS_SMC_MGMT_SDA	45 48

SMBus Charger Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
CHGR_CSI	1T01_DIFFPAIR		CHGR_CSI_P	64
	1T01_DIFFPAIR		CHGR_CSI_N	64
CHGR_CSO	1T01_DIFFPAIR		CHGR_CSO_P	64
	1T01_DIFFPAIR		CHGR_CSO_N	64

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PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
SENSE_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
THERM_1TO1_55S	*	=1:1_DIFFPAIR	=55_OHM_SE	=55_OHM_SE	=55_OHM_SE	=1:1_DIFFPAIR	=1:1_DIFFPAIR
DIFFPAIR	*	=1:1_DIFFPAIR			=1:1_DIFFPAIR	=1:1_DIFFPAIR	=1:1_DIFFPAIR

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
SENSE	*	=2:1_SPACING	?
THERM	*	=2:1_SPACING	?
AUDIO	*	=2:1_SPACING	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CPU_COMP	GND	*	GND_P2MM
CPU_VCCSENSE	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
ENETCONN	*	25 MILS	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
ENET_MDI	GND	*	GND_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND	*	=STANDARD	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
CLK_PCIE	GND	*	GND_P2MM
PCIE	GND	*	GND_P2MM
SATA	GND	*	GND_P2MM
USB	GND	*	GND_P2MM
CLK_PCIE	SB_POWER	*	PWR_P2MM
SATA	SB_POWER	*	PWR_P2MM
USB	SB_POWER	*	PWR_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
GND_P2MM	*	0.20 MM	1000
PWR_P2MM	*	0.20 MM	1000

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
MEM_CLK	GND	*	GND_P2MM
MEM_CMD	GND	*	GND_P2MM
MEM_CTRL	GND	*	GND_P2MM
MEM_DATA	GND	*	GND_P2MM
MEM_DQS	GND	*	GND_P2MM

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
LVDS	GND	*	GND_P2MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_40S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_72D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_37S OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
MEM_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
PCIE_85D OVERRIDE	* OVERRIDE	OVERRIDE	OVERRIDE	0.076 MM OVERRIDE	10 mm OVERRIDE	OVERRIDE	OVERRIDE
USB_85D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.1 MM OVERRIDE	500 MIL OVERRIDE	OVERRIDE	OVERRIDE
CPU_27P4S OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE
CLK_PCIE_90D OVERRIDE	TOP OVERRIDE	OVERRIDE	OVERRIDE	0.09 MM OVERRIDE	400 MIL OVERRIDE	OVERRIDE	OVERRIDE

Memory Constraint Relaxations

Allow 0.127 mm necks for >0.127 mm lines for ARD fanout.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
MEM_72D	BOTTOM			0.127 MM	6.35 MM		
MEM_85D	TOP			0.1 MM	6.35 MM		

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
	ENET_100D	ENETCONN	ENETCONN_P<3..0>	38
	ENET_100D	ENETCONN	ENETCONN_N<3..0>	38
	SATA_90D	SATA	SATA_ODD_D2R_UF_P	6 42
	SATA_90D	SATA	SATA_ODD_D2R_UF_N	6 42
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_P	42
	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_OUT_N	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_P	42
	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_IN_N	42
TP290	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_P	42
TP291	SATA_90D	SATA	SATA_HDD_D2R_RDRVR_IN_N	42
TP292	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_P	42
TP290	SATA_90D	SATA	SATA_HDD_R2D_RDRVR_OUT_N	42
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_P	51
	THERM_1TO1_55S	THERM	CPUTHMSNS_D2_N	51
TP287 SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	CPU_THERMD_P	9 51
TP288	THERM_1TO1_55S	THERM	CPU_THERMD_N	9 51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29_THERMD_P	34 51
	THERM_1TO1_55S	THERM	T29_THERMD_N	51
SENSE_DIFFPAIR	THERM_1TO1_55S	THERM	T29THMSNS_D2_P	51
	THERM_1TO1_55S	THERM	T29THMSNS_D2_N	51
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_COMPUTING_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_N	50
	SENSE_1TO1_55S	SENSE	ISNS_HS_OTHER_P	50
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_N	49 70
	SENSE_1TO1_55S	SENSE	CPUVCCIOS0_CS_P	49 70
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_P	49 68 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS2_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_P	49 69
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS1G_N	49 69
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUM_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_R_N	49
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_P	49
	SENSE_1TO1_55S	SENSE	CPUIMVP_ISNS_N	49
TP249 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_P	65
TP250	SENSE_1TO1_55S	SENSE	VCCSAS0_CS_N	65
TP257 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_P	68 69
TP251	SENSE_1TO1_55S	SENSE	CPUIMVP_ISUMG_N	68 69
TP253 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_CPU_N	
TP254	SENSE_1TO1_55S	SENSE	ISNS_CPU_P	
TP256 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_N	
TP255	SENSE_1TO1_55S	SENSE	ISNS_HDD_P	
TP281 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_N	
TP282	SENSE_1TO1_55S	SENSE	ISNS_HDD_R_P	
TP283 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_N	
TP284	SENSE_1TO1_55S	SENSE	ISNS_LCDBKLT_P	
TP285 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_N	
TP286	SENSE_1TO1_55S	SENSE	ISNS_ODD_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_N	
	SENSE_1TO1_55S	SENSE	ISNS_ODD_R_P	
SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_N	
	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_P	
TP292 SENSE_DIFFPAIR	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_N	
TP291	SENSE_1TO1_55S	SENSE	ISNS_P1V8GPU_R_P	
TP247	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_N	6 74
TP248	LVDS_90D	LVDS	LVDS_CONN_A_CLK_F_P	6 74

K90i Specific Net Properties

ELECTRICAL_CONSTRAINT_SET	NET_TYPE PHYSICAL	NET_TYPE SPACING		
PCIE_CLK100M_AP	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_P	6 32
	CLK_PCIE_90D	CLK_PCIE	PCIE_CLK100M_AP_CONN_N	6 32
	1TO1_DIFFPAIR		CHGR_CSI_R_P	64
	1TO1_DIFFPAIR		CHGR_CSI_R_N	64
	1TO1_DIFFPAIR		CHGR_CSO_R_P	50 64
	1TO1_DIFFPAIR		CHGR_CSO_R_N	50 64
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_P	43
(USB_EXTA)	USB_85D	USB	USB2_EXTA_MUXED_N	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_P	43
(USB_EXTA)	USB_85D	USB	USB2_LT1_N	43
	USB_85D	USB	CONN_USB2_BT_P	
	USB_85D	USB	CONN_USB2_BT_N	
	USB_85D	USB	USB_LT2_P	43
	USB_85D	USB	USB_LT2_N	43
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_P	
	DP_85D	DISPLAYPORT	DP_IG_AUX_CH_C_N	
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_L_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_SUB_N_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_P_OUT	6 60 61
SPK_OUT	DIFFPAIR	AUDIO	SPKRAMP_R_N_OUT	6 60 61
TP395 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_N	60
TP396 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_SUB_P	60
TP397 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_N	60
TP398 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_L_P	60
TP399 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_N	60
TP400 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SSM2315_R_P	60
TP406 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_R	57 60
TP407 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_R	57 60
TP408 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_N_R	57 60
TP410 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO1_P_R	57 60
TP409 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_N_L	57 60
TP390 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	AUD_LO2_P_L	57 60
TP414 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_P	60
TP415 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INL_N	60
TP413 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_P	60
TP412 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INR_N	60
TP416 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_P	60
TP417 AUD_DIFF	1TO1_DIFFPAIR	AUDIO	SPKRAMP_INSUB_N	60
	USB_85D	USB	USB_TPAD_R_P	53
	USB_85D	USB	USB_TPAD_R_N	53
		SB_POWER	PP3V3_S5	6 7 8 12 16 19 20 22 23 24 26 30 40 58 72 73 74 76 48 49 50
		SB_POWER	PP3V3_S0	6 7 8 12 16 17 18 19 20 22 23 26 27 29 33 36 37 40 41 52 54
		SB_POWER	PP1V5_S3RS0	6 7 10 12 15 30 72 73 57 61 62 71 73 74 77
		GND	GND	

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Project Specific Constraints

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K90i Board-Specific Spacing & Physical Constraints

BOARD LAYERS	BOARD AREAS	BOARD UNITS (MIL or MM)	ALLEGRO VERSION
TOP,ISL2,ISL3,ISL4,ISL5,ISL6,ISL7,ISL8,ISL9,ISL10,ISL11,BOTTOM	NO_TYPE,BGA	MM	15.5.1

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
DEFAULT	*	Y	=50_OHM_SE	=50_OHM_SE	10 MM	0 MM	0 MM
STANDARD	*	Y	=DEFAULT	=DEFAULT	10 MM	=DEFAULT	=DEFAULT

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
50_OHM_SE	TOP,BOTTOM	Y	0.110 MM	0.090 MM			
50_OHM_SE	*	Y	0.080 MM	0.080 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
40_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
40_OHM_SE	ISL10	N	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	ISL3,ISL4,ISL9	Y	0.126 MM	0.126 MM	=STANDARD	=STANDARD	=STANDARD
40_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
37_OHM_SE	TOP,BOTTOM	Y	0.190 MM	0.1 MM			
37_OHM_SE	ISL10	N	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	ISL3,ISL4,ISL9	Y	0.145 MM	0.1 MM	=STANDARD	=STANDARD	=STANDARD
37_OHM_SE	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
27P4_OHM_SE	TOP,BOTTOM	Y	0.310 MM	0.2 MM			
27P4_OHM_SE	*	Y	0.235 MM	0.2 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
55_OHM_SE	TOP,BOTTOM	Y	0.090 MM	0.090 MM			
55_OHM_SE	*	Y	0.070 MM	0.070 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
72_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
72_OHM_DIFF	ISL3,ISL4,ISL9	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	ISL10	N	0.140MM	0.140 MM		0.190 MM	0.190 MM
72_OHM_DIFF	TOP,BOTTOM	Y	0.175 MM	0.175 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
85_OHM_DIFF	ISL3,ISL4	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	ISL9,ISL10	Y	0.101 MM	0.1 MM		0.170 MM	0.170 MM
85_OHM_DIFF	TOP,BOTTOM	Y	0.125 MM	0.1 MM		0.190 MM	0.190 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
90_OHM_DIFF	ISL3,ISL4	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	ISL9,ISL10	Y	0.091 MM	0.091 MM		0.180 MM	0.180 MM
90_OHM_DIFF	TOP,BOTTOM	Y	0.111 MM	0.111 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
100_OHM_DIFF	ISL3,ISL4	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	ISL9,ISL10	Y	0.076 MM	0.076 MM		0.250 MM	0.250 MM
100_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.200 MM	0.200 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
110_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
110_OHM_DIFF	ISL3,ISL4	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	ISL9,ISL10	Y	0.070 MM	0.070 MM		0.330 MM	0.330 MM
110_OHM_DIFF	TOP,BOTTOM	Y	0.085 MM	0.085 MM		0.250 MM	0.250 MM

NOTE: These are Intel recommended impedances for PEG, unused on K90i.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
48_OHM_SE	TOP,BOTTOM	Y	0.165 MM	0.165 MM			
48_OHM_SE	*	Y	0.090 MM	0.090 MM	=STANDARD	=STANDARD	=STANDARD

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
80_OHM_DIFF	*	N	=STANDARD	=STANDARD	=STANDARD	=STANDARD	=STANDARD
80_OHM_DIFF	ISL3,ISL4	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	ISL9,ISL10	Y	0.115 MM	0.115 MM		0.180 MM	0.180 MM
80_OHM_DIFF	TOP,BOTTOM	Y	0.140 MM	0.140 MM		0.190 MM	0.190 MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
DEFAULT	*	0.1 MM	?
STANDARD	*	=DEFAULT	?
BGA_P1MM	*	=DEFAULT	?
BGA_P2MM	*	=DEFAULT	?

NET_SPACING_TYPE1	NET_SPACING_TYPE2	AREA_TYPE	SPACING_RULE_SET
*	*	BGA	BGA_P1MM
MEM_CLK	*	BGA	BGA_P2MM
CLK_PCIE	*	BGA	BGA_P2MM
CLK_SLOW	*	BGA	BGA_P2MM

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
1.5:1_SPACING	*	0.15 MM	?
2:1_SPACING	*	0.2 MM	?
2.5:1_SPACING	*	0.25 MM	?
3:1_SPACING	*	0.3 MM	?
4:1_SPACING	*	0.4 MM	?

SPACING_RULE_SET	LAYER	LINE-TO-LINE SPACING	WEIGHT
2X_DIELECTRIC	*	0.140 MM	?
3X_DIELECTRIC	*	0.210 MM	?
4X_DIELECTRIC	*	0.280 MM	?
5X_DIELECTRIC	*	0.350 MM	?
7X_DIELECTRIC	*	0.490 MM	?

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
1:1_DIFFPAIR	*	Y	=STANDARD	=STANDARD	=STANDARD	0.1 MM	0.1 MM

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
85_DIFF_BGA	*	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF	=85_OHM_DIFF
85_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
85_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 85_DIFF_BGA is 85-ohms differential impedance on outer layers and 80-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
90_DIFF_BGA	*	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF	=90_OHM_DIFF
90_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
90_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 90_DIFF_BGA is 90-ohms differential impedance on outer layers and 85-ohms on inner layers.

PHYSICAL_RULE_SET	LAYER	ALLOW ROUTE ON LAYER?	MINIMUM LINE WIDTH	MINIMUM NECK WIDTH	MAXIMUM NECK LENGTH	DIFFPAIR PRIMARY GAP	DIFFPAIR NECK GAP
100_DIFF_BGA	*	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF	=100_OHM_DIFF
100_DIFF_BGA	ISL3,ISL4	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM
100_DIFF_BGA	ISL9,ISL10	Y	0.075 MM	0.075 MM		0.125 MM	0.125 MM

NOTE: 100_DIFF_BGA is 100-ohms differential impedance on outer layers and 95-ohms on inner layers.

NOTE: 110_DIFF is 110-ohms differential impedance on outer layers and 105-ohms on inner layers.

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